

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD DATE
0.1	0010932459	ENGINEERING RELEASED	06/04/2014

## SCHEM, MLB, VENUS2, PROTO1A

ENG

06/04/2014

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
VENUS2, PROTO1A : PRELIMINARY  
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Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-00388	1	SCHEM,MLB,VENUS2,PROTO1A	SCH	CRITICAL	
820-00426	1	PCBF,MLB,VENUS2,PROTO1A	PCB	CRITICAL	

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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
685-00042	COMMON PARTS,MLB,VENUS2	X425_COMMON
985-00050	DEV BOM,MLB,VENUS2	X425_DEVEL:ENG
639-00682	PCBA,MLB,VENUS2,CTO,16GHYN,VR-4GHYN,X425G	BASE_BOM,DEVEL_BOM,GFX_BOM,CPU_CRW:CTO,RAM:HYNIX_1600,FB_4G_HYNIX
639-00703	PCBA,MLB,VENUS2,CTO,16GMIC,VR-4GMIC,X425G	BASE_BOM,DEVEL_BOM,GFX_BOM,CPU_CRW:CTO,RAM:MICRON_1600,FB_4G_MICRON
639-00739	PCBA,MLB,VENUS2,CTO,16GHYN,VR-4GMIC,X425G	BASE_BOM,DEVEL_BOM,GFX_BOM,CPU_CRW:CTO,RAM:HYNIX_1600,FB_4G_MICRON
639-00740	PCBA,MLB,VENUS2,CTO,16GMIC,VR-4GHYN,X425G	BASE_BOM,DEVEL_BOM,GFX_BOM,CPU_CRW:CTO,RAM:MICRON_1600,FB_4G_HYNIX
639-00798	PCBA,MLB,VENUS2,BEST,16GHYN,VR-4GHYN,X425G	BASE_BOM,DEVEL_BOM,GFX_BOM,CPU_CRW:BEST,RAM:HYNIX_1600,FB_4G_HYNIX
639-00799	PCBA,MLB,VENUS2,BEST,16GMIC,VR-4GMIC,X425G	BASE_BOM,DEVEL_BOM,GFX_BOM,CPU_CRW:BEST,RAM:MICRON_1600,FB_4G_MICRON
639-00800	PCBA,MLB,VENUS2,BEST,16GHYN,VR-4GMIC,X425G	BASE_BOM,DEVEL_BOM,GFX_BOM,CPU_CRW:BEST,RAM:HYNIX_1600,FB_4G_MICRON
639-00801	PCBA,MLB,VENUS2,BEST,16GMIC,VR-4GHYN,X425G	BASE_BOM,DEVEL_BOM,GFX_BOM,CPU_CRW:BEST,RAM:MICRON_1600,FB_4G_HYNIX
639-00803	PCBA,MLB,VENUS2,NOCPU,16GMIC,VR-4GHYN,X425G	BASE_BOM,DEVEL_BOM,GFX_BOM,RAM:MICRON_1600,FB_4G_HYNIX
639-00974	PCBA,MLB,NOGPU,CTO,16GMIC,VR-4GHYN,X425G	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:MICRON_1600,FB_4G_HYNIX

X425 BOM Groups

BOM GROUP	BOM OPTIONS
X425_COMMON	ALTERNATE,COMMON,X425_COMMON1,X425_COMMON2,X425_PROGPARTS,ACAPS:A2
X425_COMMON1	CPUMEM:S0,TBTHV:P15V,SKIP_5V3V3:AUDIBLE,CPUPEG:X8X4X4,S2_PWR:S0,SMC_SUSACK:YES
X425_COMMON2	EDP:YES,XDP,SSD_PWR_EN:GPIO,CAM_WAKE:NO,SAMCONN,APCLKRQ:ISOL,CRW_SPRT,WLAN_SW:SIL
X425_PVT	BKLT:PROD,SENSOR_NONPROD:N
X425_PROGPARTS	SMC_PROG:BASE,BOOTROM_PROG:EVT,TBTROM:PROG,DPMUXMCU:PROG
X425_DEVEL:ENG	ALTERNATE,XDP_DEBUG,SOPGOOD_ISL,SENSOR_NONPROD:Y,SENSOR_NONPROD_R,BKLT:ENG,DBGLED,DPMUX_DEBUG,GPU_ROM:YES,SENSOR_GPU_NONPROD:Y
X425_DEVEL:DVT	ALTERNATE,XDP_DEBUG,BKLT:PROD,SENSOR_NONPROD:N,DBGLED
X425_DEVEL:PVT	XDP_DEBUG
GFX_BOM	VENUS:XTA
XDP_DEBUG	XDP_CONN,XDP_PCH

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S00058	1	CRW,SR1ZX,PRQ,C0,2.5,47W,4+3E,1.2,6M,BGA	U0500	CRITICAL	CPU_CRW:BEST
337S00059	1	CRW,SR1ZY,PRQ,C0,2.5,47W,4+3E,1.2,6M,BGA	U0500	CRITICAL	CPU_CRW:CTO
337S4542	1	IC,QEWV,LPT-R,RMB7,C2,SR199,PRQ,PCBGA	U1100	CRITICAL	
338S1247	1	IC,TBT,FR-4C,A0,PRQ,CIO,SR1JC,PCBGA288	U2800	CRITICAL	
338S1264	1	IC,BCH15700A2,S2 PCIE CHRA,8X8,208PFBGA	U3900	CRITICAL	
333S0700	1	IC,SDRAM,4GBIT,DDR3L-1600,GE9MA,96B FBGA	U4000	CRITICAL	
333S00032	32	IC,SDRAM,DDR3L-1600,4GBIT,78B FBGA		CRITICAL	HYNIX_1600
333S0660	32	IC,SDRAM,4GBIT,DDR3L-1600,V80A,78P,FBGA		CRITICAL	MICRON_1600
337S00116	1	IC,GPU,VENUS XTA1.Q8,29X29MM,PCBGA962	U8400	CRITICAL	VENUS:XTA
333S00027	4	IC,ODDS,4GBIT,6GBPS,1.5V,25MM,BGA170	U8800,U8850,U8900,U8950	CRITICAL	FB_4G_HYNIX
333S0766	4	IC,ODDS,4GBIT,6GBPS,128MX32,25MM,170BGA	U8800,U8850,U8900,U8950	CRITICAL	FB_4G_MICRON

VENUS2, PROTO1A : PRELIMINARY  
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DRAM SPD Straps

BOM GROUP	BOM OPTIONS
RAM:HYNIX_1600	HYNIX_1600,RAMCFG3:H,RAMCFG2:H,RAMCFG1:L,RAMCFG0:L
RAM:MICRON_1600	MICRON_1600,RAMCFG3:H,RAMCFG2:H,RAMCFG1:H,RAMCFG0:L


COMMON/DEVEL BOM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
685-00042	1	COMMON PARTS,MLB,VENUS,X425G	BASE	CRITICAL	BASE_BOM
985-00050	1	DEV,MLB,VENUS,X425G	DEVEL	CRITICAL	DEVEL_BOM

SYNC MASTER=CLEAN X305

SYNC DATE=05/30/2014

BOM Configuration

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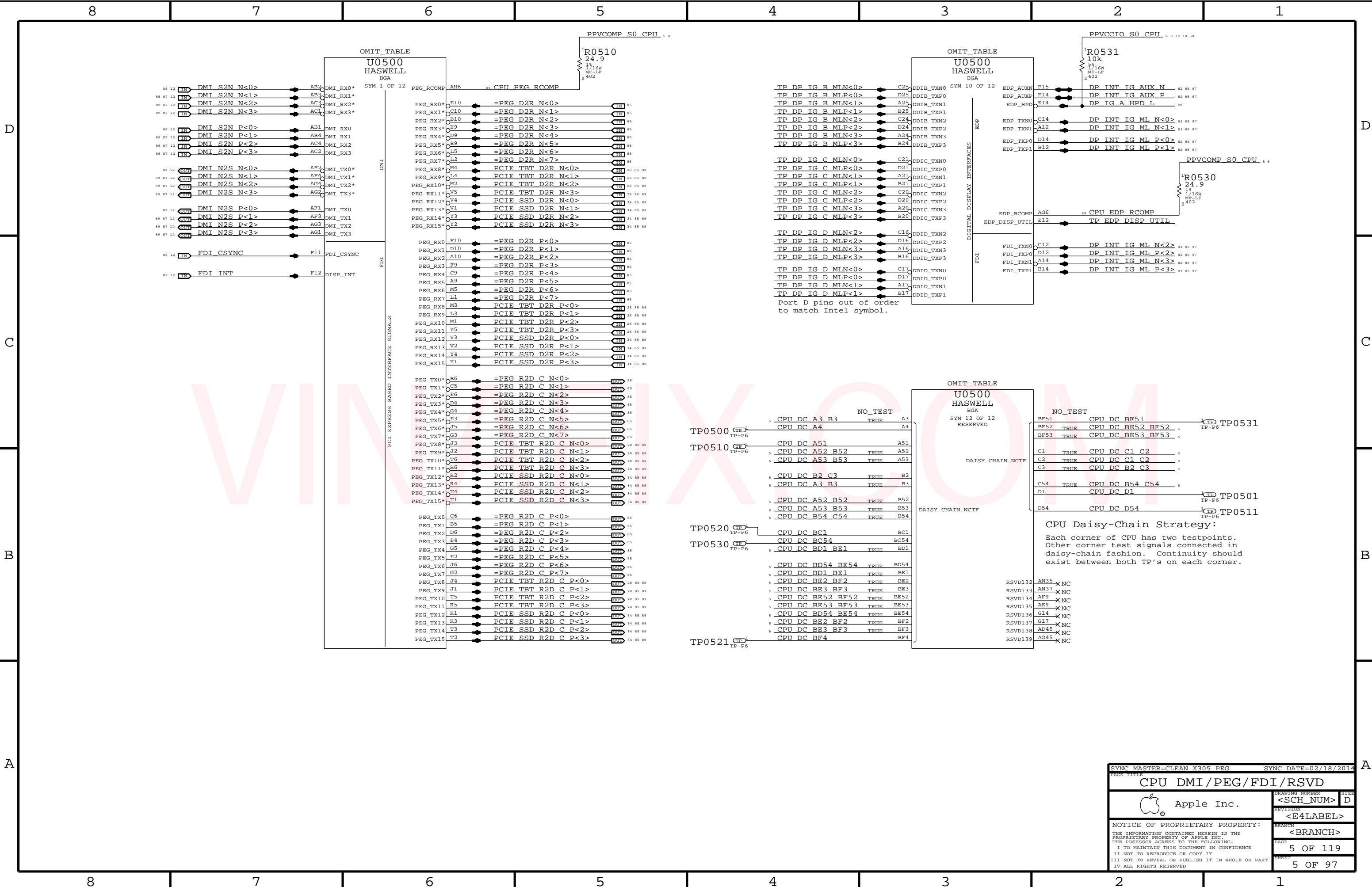
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SYNC MASTER=CLEAN X305 PEG

SYNC DATE=02/18/2014

CPU DMI / PEG / FDI / RSVD

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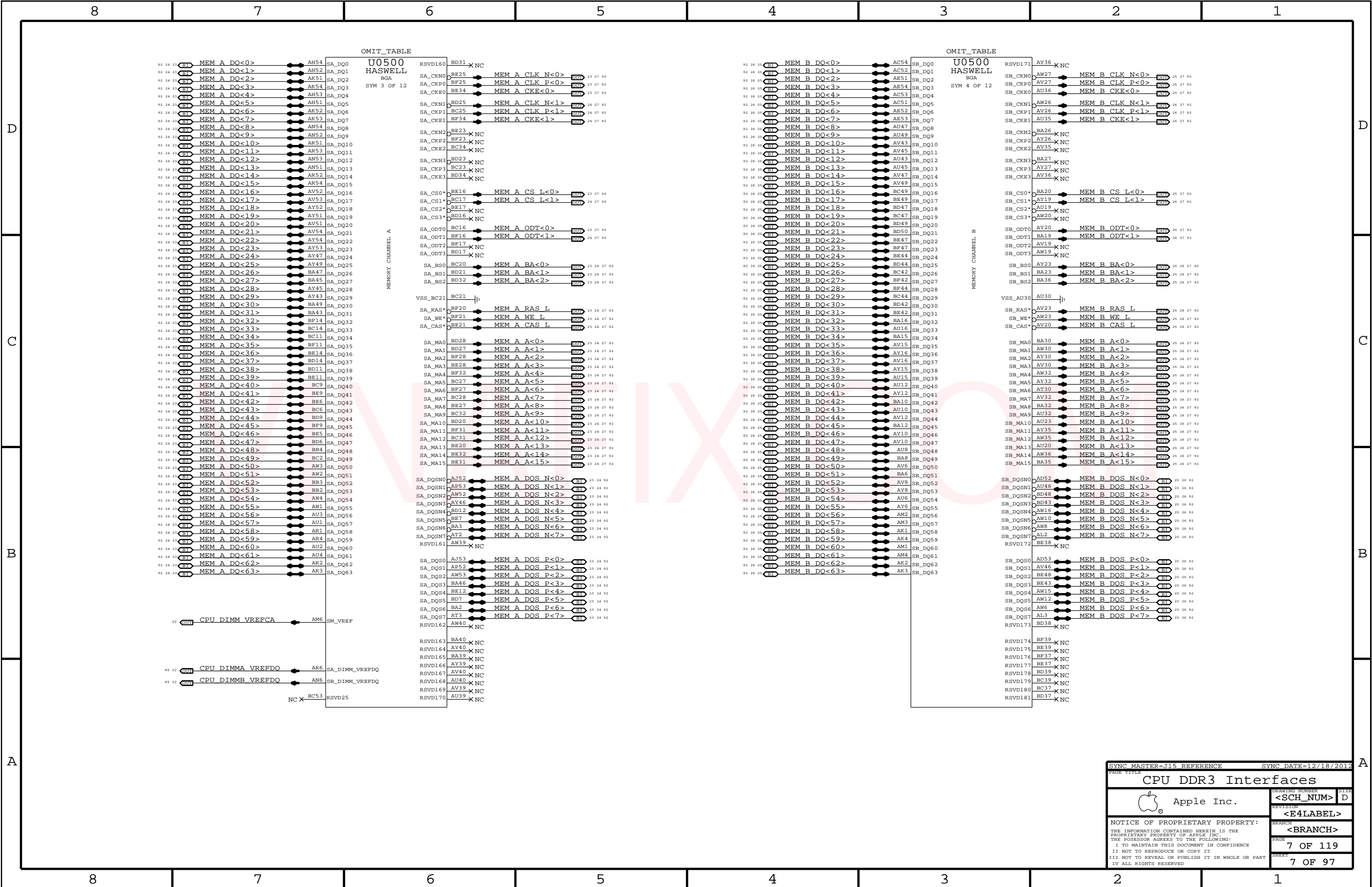
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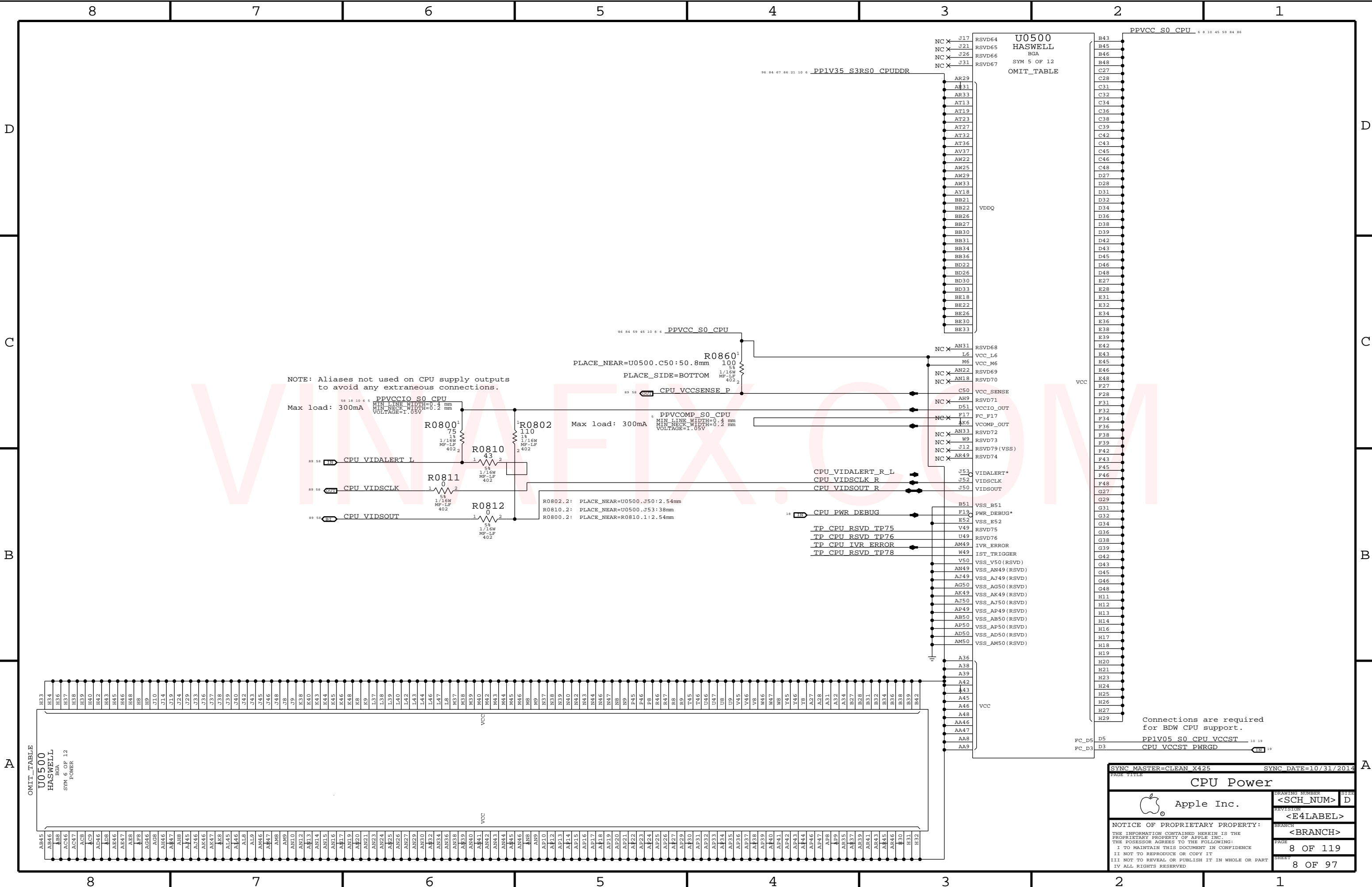
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NOTE: Aliases not used on CPU supply outputs to avoid any extraneous connections.

Max load: 300mA  
PPVCCIO S0 CPU  
MIN LINE WIDTH=0.4 mm  
MIN NECK WIDTH=0.2 mm  
VOLTAGE=1.05V

PLACE\_NEAR=U0500.C50:50.8mm  
PLACE\_SIDE=BOTTOM  
PPVCC S0 CPU  
CPU VCCSENSE P  
PPVCOMP S0 CPU  
Max load: 300mA  
MIN LINE WIDTH=0.4 mm  
MIN NECK WIDTH=0.2 mm  
VOLTAGE=1.05V

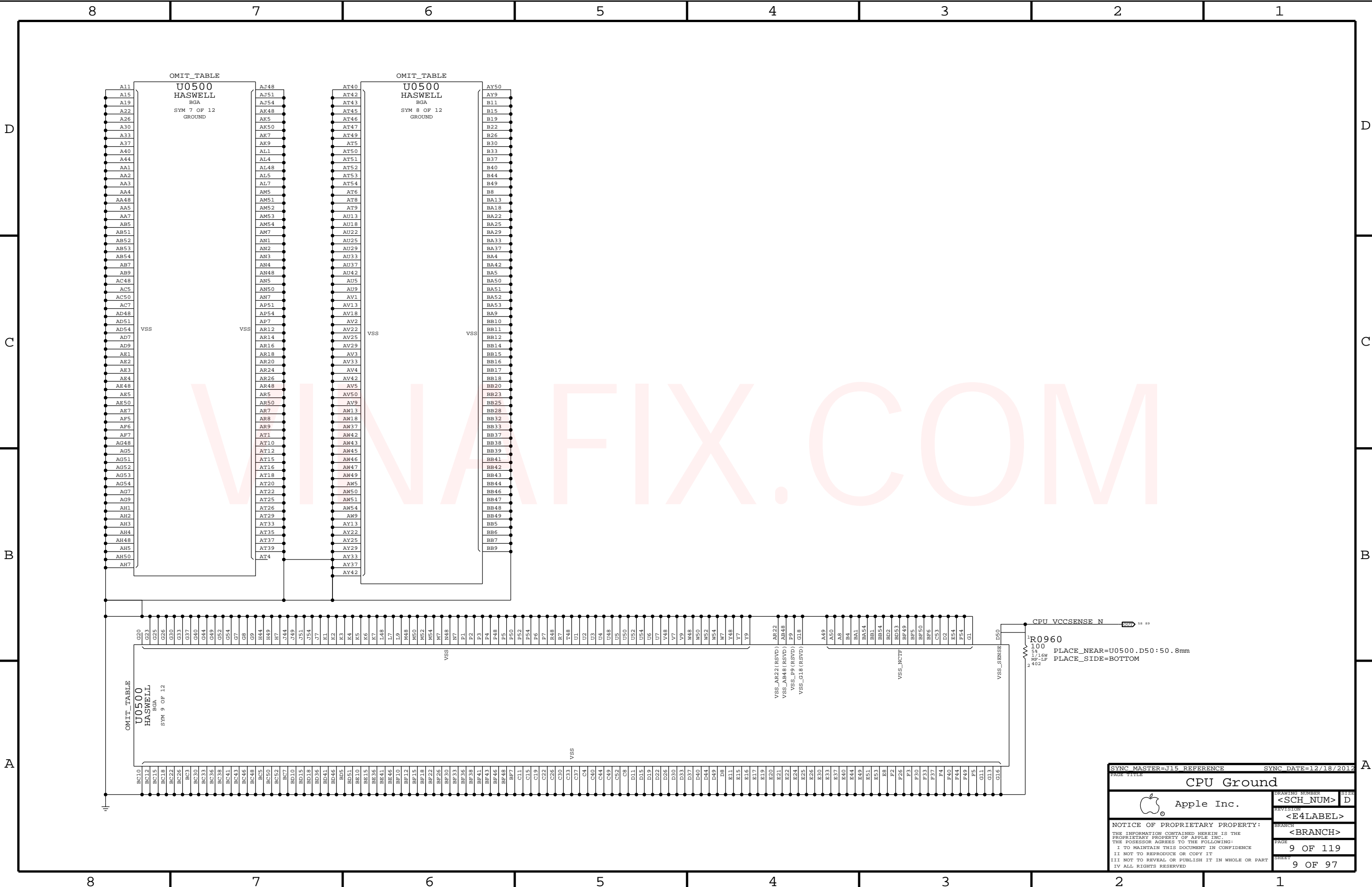
R0802.2: PLACE\_NEAR=U0500.J50:2.54mm  
R0810.2: PLACE\_NEAR=U0500.J53:38mm  
R0800.2: PLACE\_NEAR=R0810.1:2.54mm

Connections are required for BDW CPU support.

FC\_D5 D5 PP1V05 S0 CPU VCCST 10 19  
FC\_D3 D3 CPU VCCST PWRGD 19

SYNC MASTER=CLEAN X425		SYNC DATE=10/31/2014	
CPU Power			
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## CPU VCORE Decoupling

Intel recommendation: 4x 470uF 4mOhm (3 CPU-side, 1 opposite), 20x 22uF 0805 (10 CPU-side, 10 opposite near edge), 4x 10uF 0603 (2 CPU-side, 2 opposite), 20x 1uF 0402 (under CPU)  
Apple Implementation: 9x 210uF 6mOhm, 44x 10uF 0402, 4x 10uF 0402, 20x 1uF 0402

PLACEMENT\_NOTE (C1000-C1019):

Place on bottom side of U0500

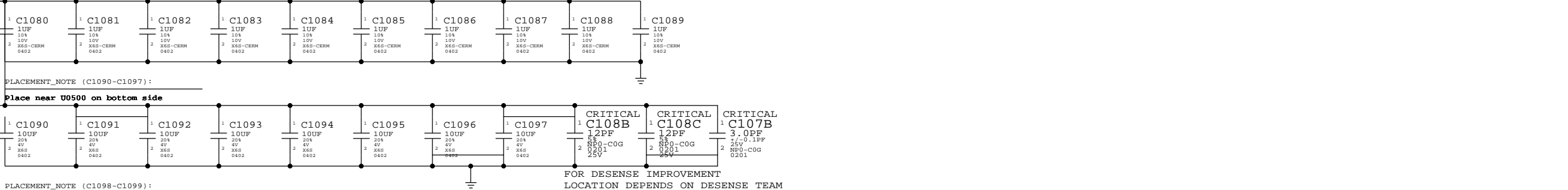


## CPU VDDQ Decoupling

Intel recommendation: 2x 330uF, 8x 10uF 0603, 10x 1uF 0402  
Apple Implementation: 3x 270uF, 8x 10uF 0603, 10x 1uF 0402

PLACEMENT\_NOTE (C1080-C1089):

Place on bottom side of U0500



## CPU VCCIO Decoupling

Intel recommendation: 2x 0.01uF 0402 (1 near CPU, 1 near SVID pull-ups)  
Apple Implementation: 2x 0.01uF 0402 (second cap is on CPU VR page)

PLACEMENT\_NOTE (C1098-C1099):

Place on bottom side of U0500

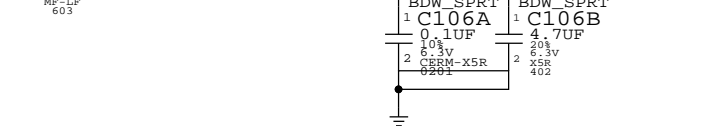


## CPU VCCST Decoupling

BDW\_SPRT Intel recommendation: 1x 0.1uF 0402, 1x 4.7uF 0805  
R1080 Apple Implementation: 1x 0.1uF 0201, 1x 4.7uF 0402

PLACEMENT\_NOTE (C106A-C106B):


Place near U0500.D5:12.7mm

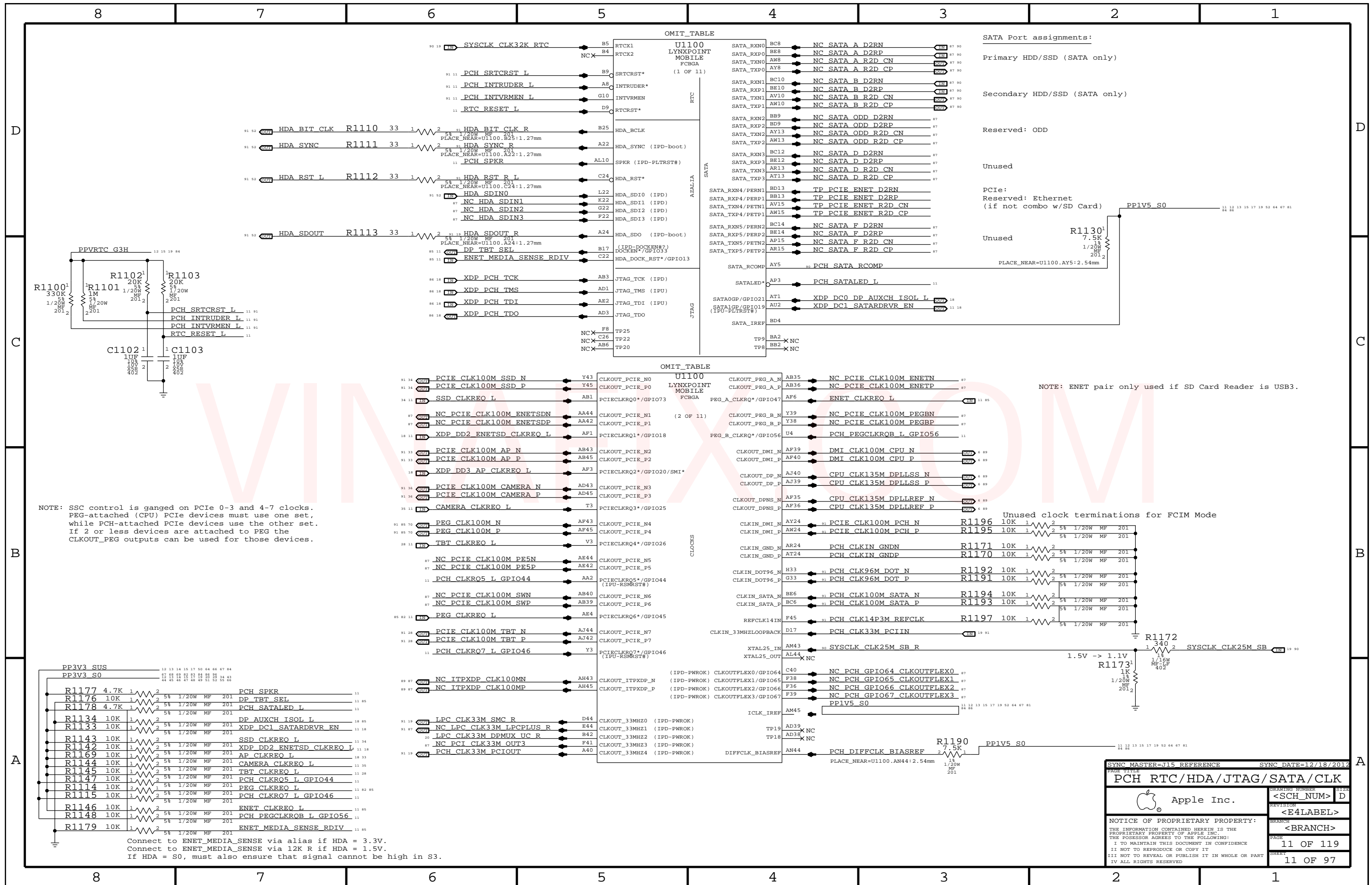


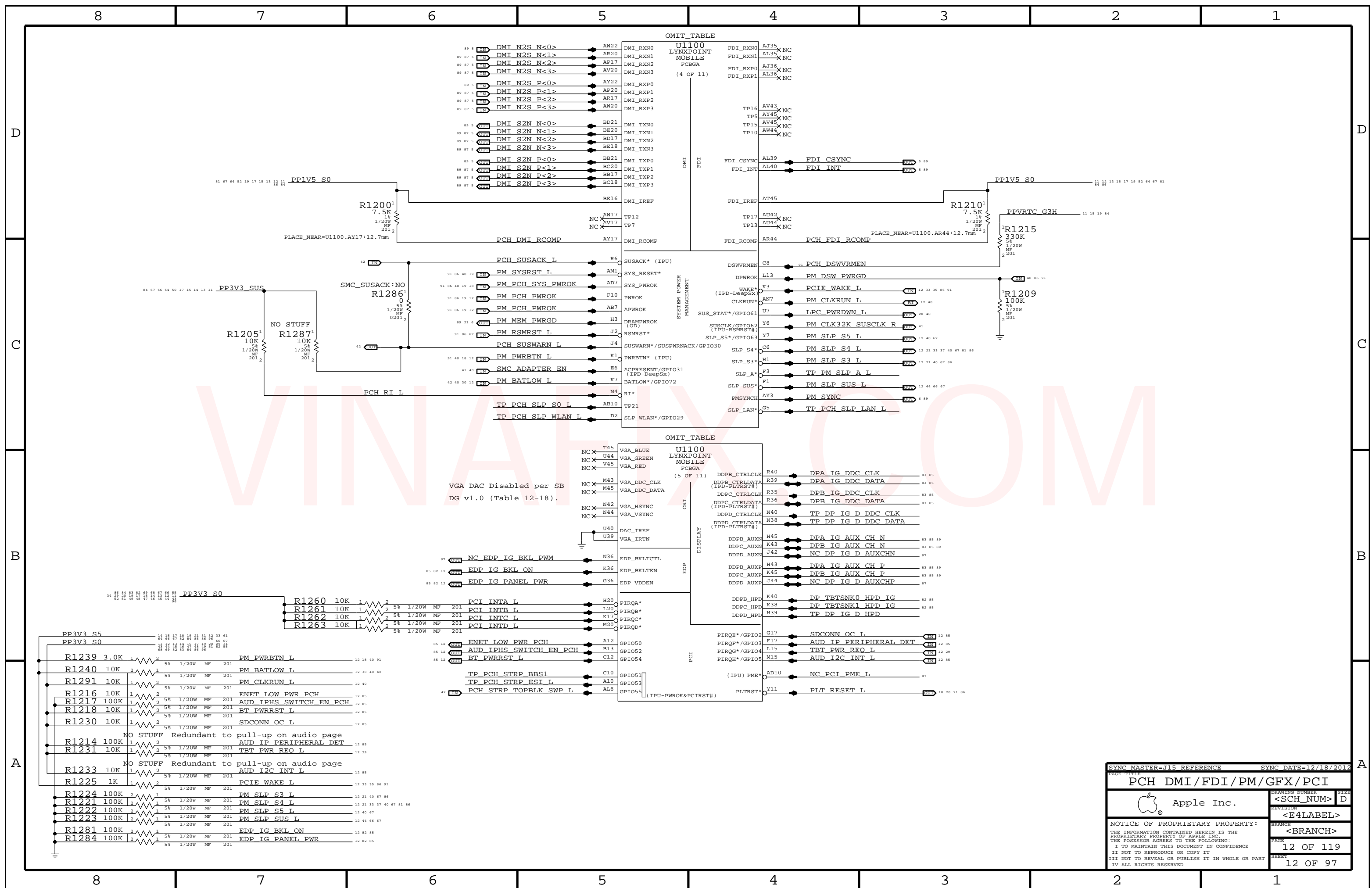
FOR DESENSE IMPROVEMENT  
LOCATION DEPENDS ON DESENSE TEAM

FOR DESENSE IMPROVEMENT  
LOCATION DEPENDS ON DESENSE TEAM

C1098, C1099 and C108A use B size caps due to EG board placement constraints.

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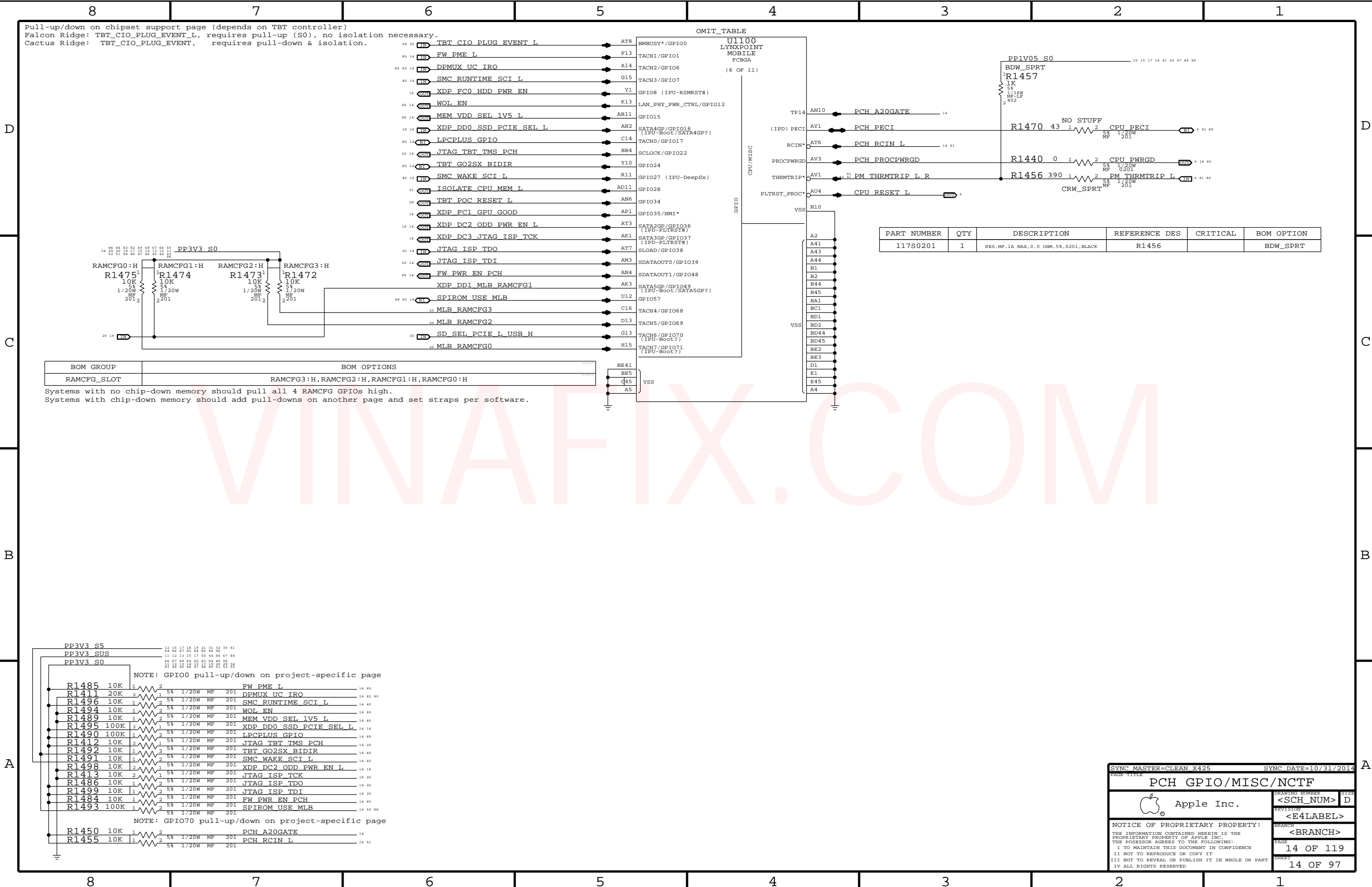






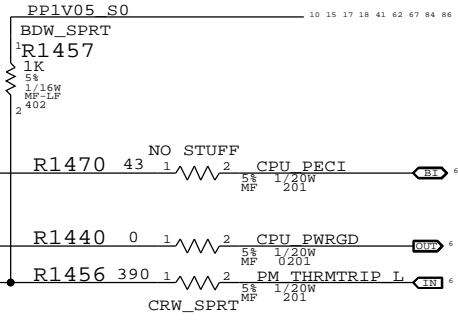






Pull-up/down on chipset support page (depends on TBT controller)  
Falcon Ridge: TBT\_CIO\_PLUG\_EVENT\_L, requires pull-up (S0), no isolation necessary.  
Cactus Ridge: TBT\_CIO\_PLUG\_EVENT, requires pull-down & isolation.

OMIT\_TABLE  
U1100  
LYNXPPOINT  
MOBILE  
FCBGA  
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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0201	1	RES,MF,1A MAX,0.0 OHM,5%,0201,BLACK	R1456		BDW_SPRT

BOM GROUP	BOM OPTIONS
RAMCFG_SLOT	RAMCFG3:H, RAMCFG2:H, RAMCFG1:H, RAMCFG0:H

Systems with no chip-down memory should pull all 4 RAMCFG GPIOs high.  
Systems with chip-down memory should add pull-downs on another page and set straps per software.

NOTE: GPIO0 pull-up/down on project-specific page

NOTE: GPIO70 pull-up/down on project-specific page

SYNC MASTER=CLEAN X425

SYNC DATE=10/31/2014

PCH GPIO/MISC/NCTF

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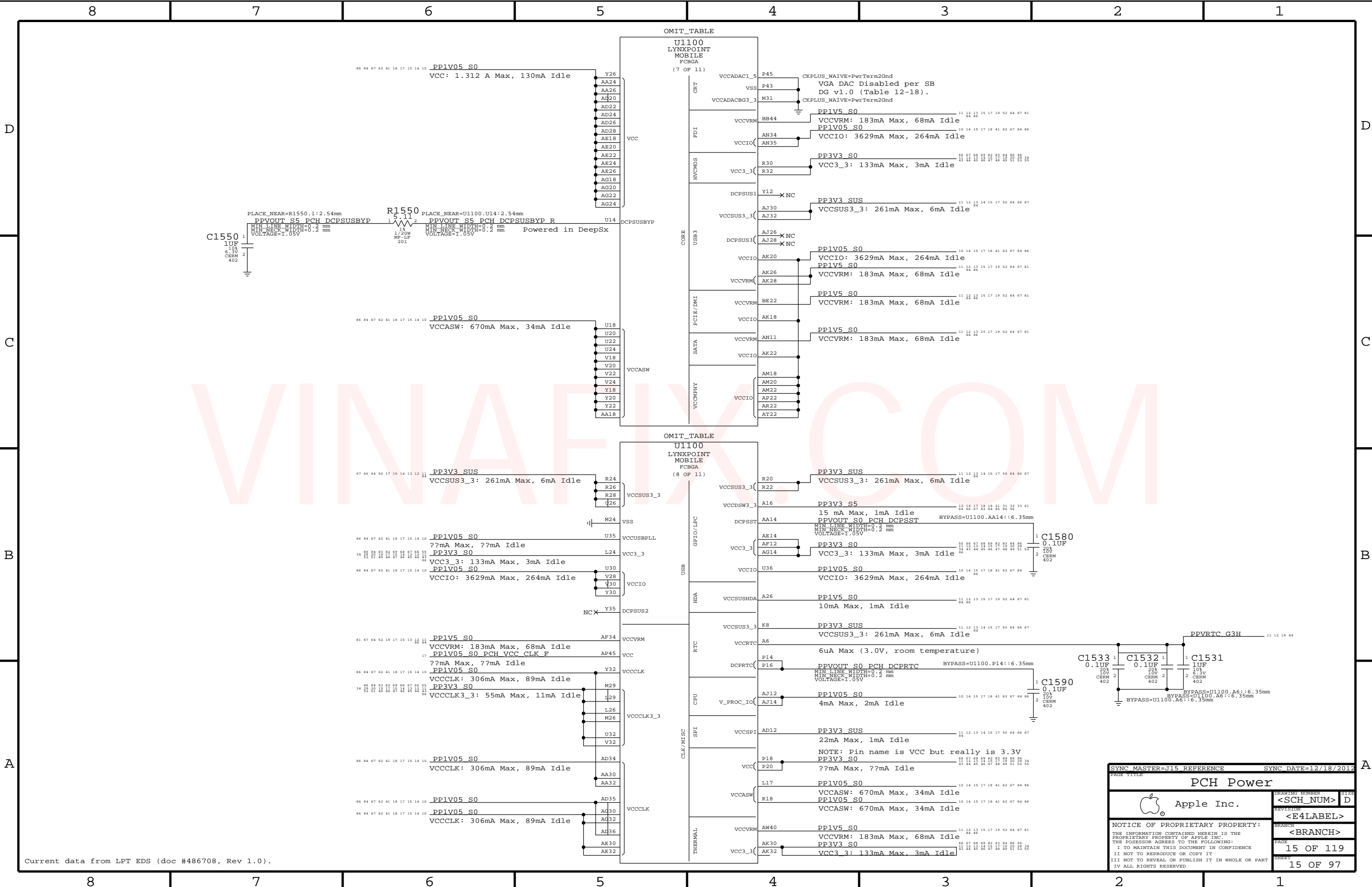
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
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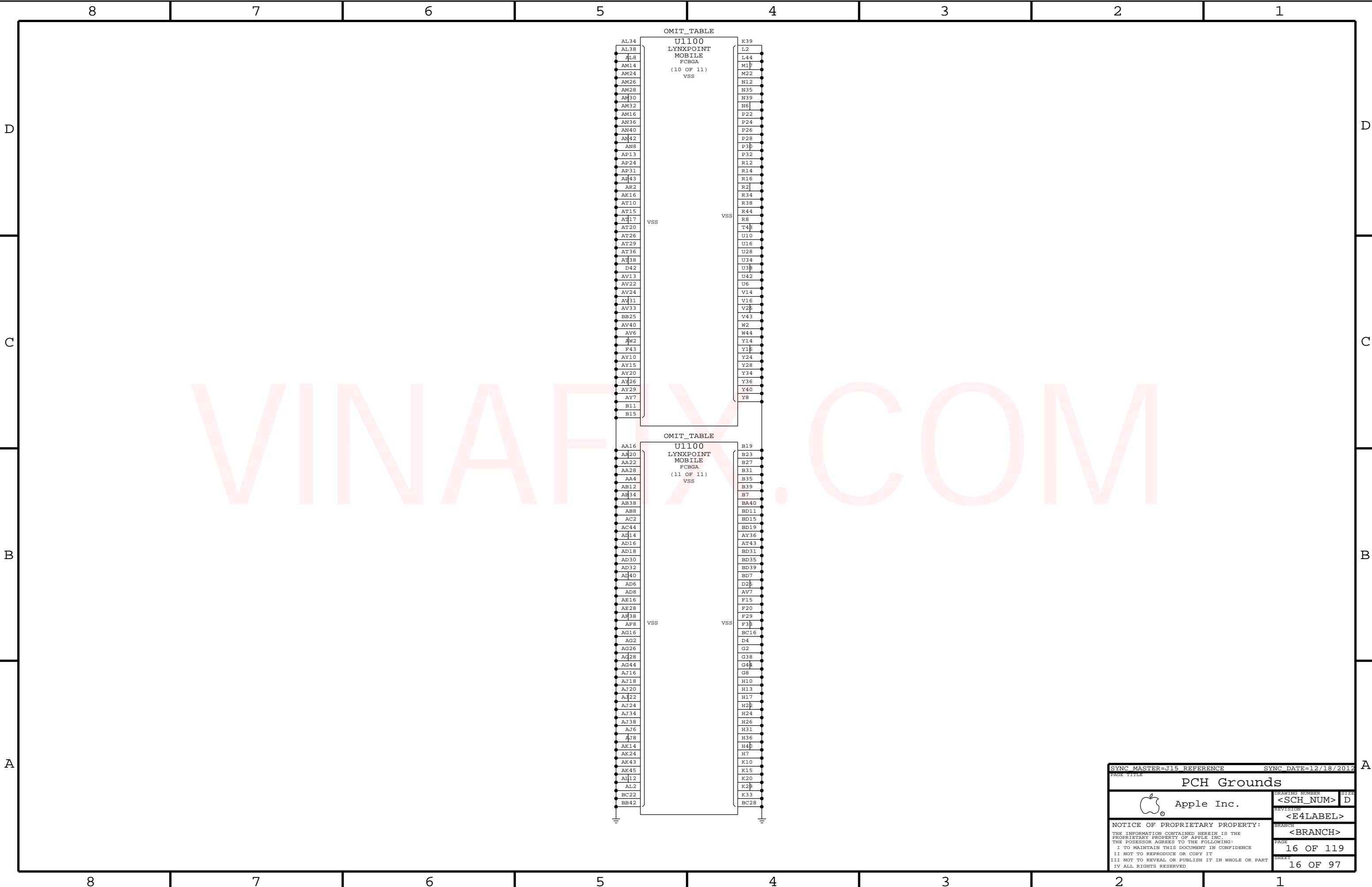
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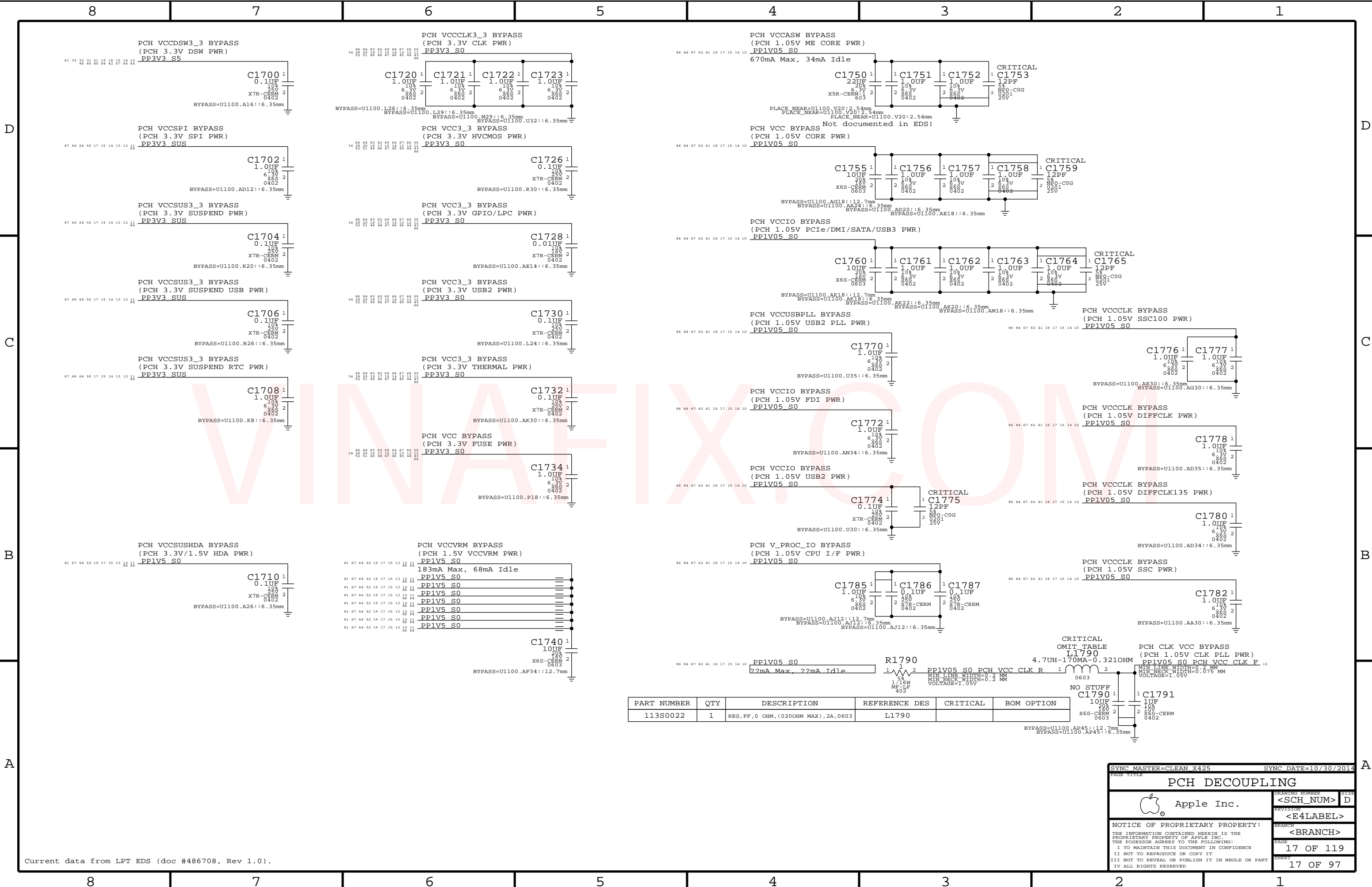


Current data from LPT EDS (doc #486708, Rev 1.0).

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SYNC DATE=10/30/2014

PCH DECOUPLING

Apple Inc.

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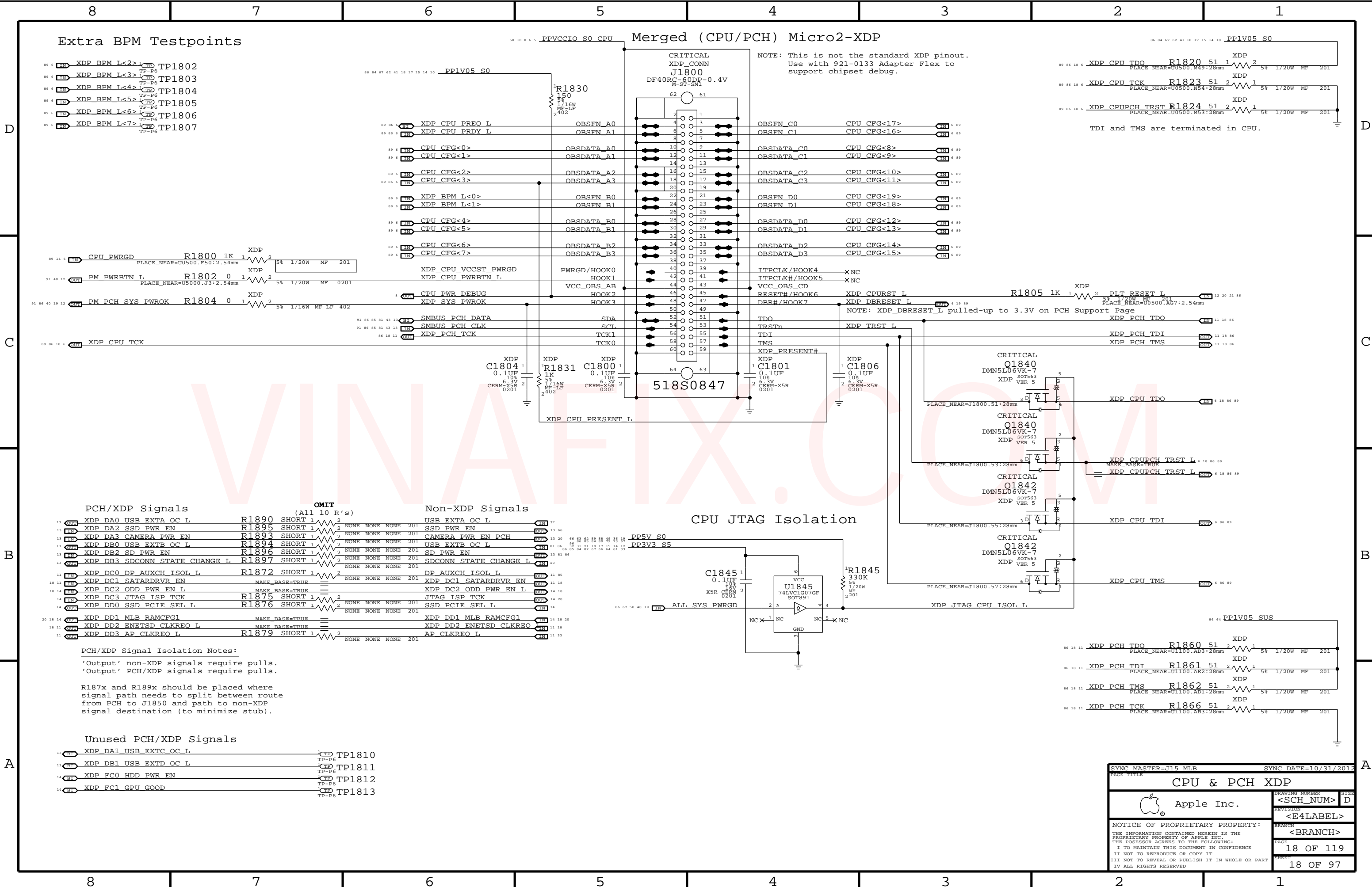
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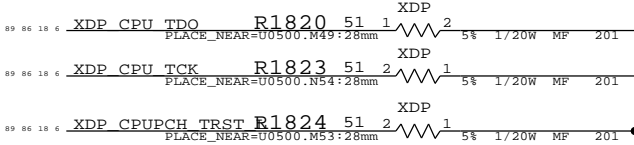
Extra BPM Testpoints

- XDP BPM L<2> TP1802
- XDP BPM L<3> TP1803
- XDP BPM L<4> TP1804
- XDP BPM L<5> TP1805
- XDP BPM L<6> TP1806
- XDP BPM L<7> TP1807

Merged (CPU/PCH) Micro2-XDP

NOTE: This is not the standard XDP pinout. Use with 921-0133 Adapter Flex to support chipset debug.

PP1V05 S0



TDI and TMS are terminated in CPU.

PCH/XDP Signals

PCH/XDP Signals		Non-XDP Signals	
XDP DA0 USB EXTA OC L	R1890 SHORT 1	USB EXTA OC L	TP1810
XDP DA2 SSD PWR EN	R1895 SHORT 1	SSD PWR EN	TP1811
XDP DA3 CAMERA PWR EN	R1893 SHORT 1	CAMERA PWR EN PCH	TP1812
XDP DB0 USB EXTB OC L	R1894 SHORT 1	USB EXTB OC L	TP1813
XDP DB2 SD PWR EN	R1896 SHORT 1	SD PWR EN	
XDP DB3 SDCONN STATE CHANGE L	R1897 SHORT 1	SDCONN STATE CHANGE L	
XDP DC0 DP AUXCH ISOL L	R1872 SHORT 1	DP AUXCH ISOL L	
XDP DC1 SATARDVR EN	MAKE_BASE=TRUE	XDP DC1 SATARDVR EN	
XDP DC2 ODD PWR EN L	MAKE_BASE=TRUE	XDP DC2 ODD PWR EN L	
XDP DC3 JTAG ISP TCK	R1875 SHORT 1	JTAG ISP TCK	
XDP DD0 SSD PCIE SEL L	R1876 SHORT 1	SSD PCIE SEL L	
XDP DD1 MLB RAMCFG1	MAKE_BASE=TRUE	XDP DD1 MLB RAMCFG1	
XDP DD2 ENETSD CLKREQ L	MAKE_BASE=TRUE	XDP DD2 ENETSD CLKREQ L	
XDP DD3 AP CLKREQ L	R1879 SHORT 1	AP CLKREQ L	

PCH/XDP Signal Isolation Notes:

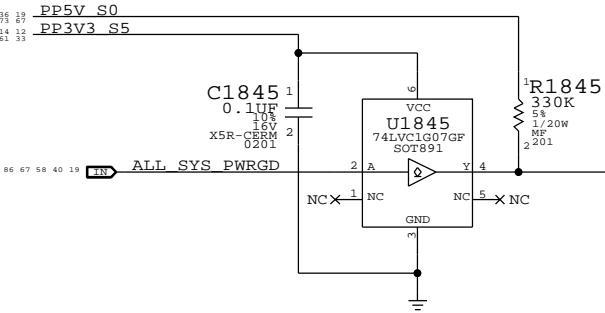
- 'Output' non-XDP signals require pulls.
- 'Output' PCH/XDP signals require pulls.


R187x and R189x should be placed where signal path needs to split between route from PCH to J1850 and path to non-XDP signal destination (to minimize stub).

Unused PCH/XDP Signals

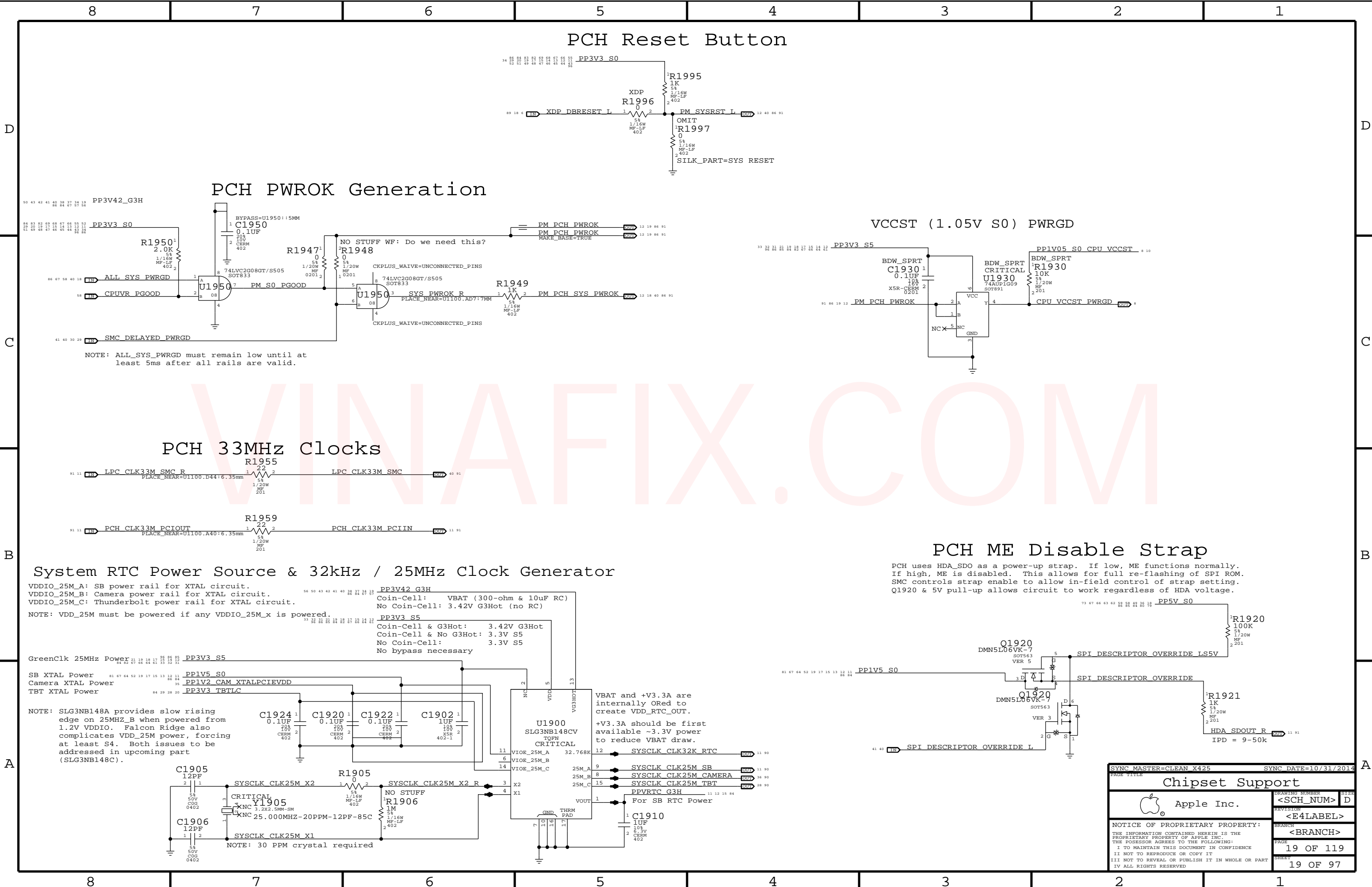
- XDP DA1 USB EXTC OC L TP1810
- XDP DB1 USB EXTD OC L TP1811
- XDP FC0 HDD PWR EN TP1812
- XDP FC1 GPU GOOD TP1813

CPU JTAG Isolation



SYNC MASTER=J15 MLB		SYNC DATE=10/31/2012	
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CPU & PCH XDP			
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Apple Inc.		<SCH_NUM>	D
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## D



The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM\_DRAMRST# output from the SO-DIMMs when necessary.

ISOLATE\_CPU\_MEM\_L GPIO state during S3->S0 transitions determines behavior of signals.

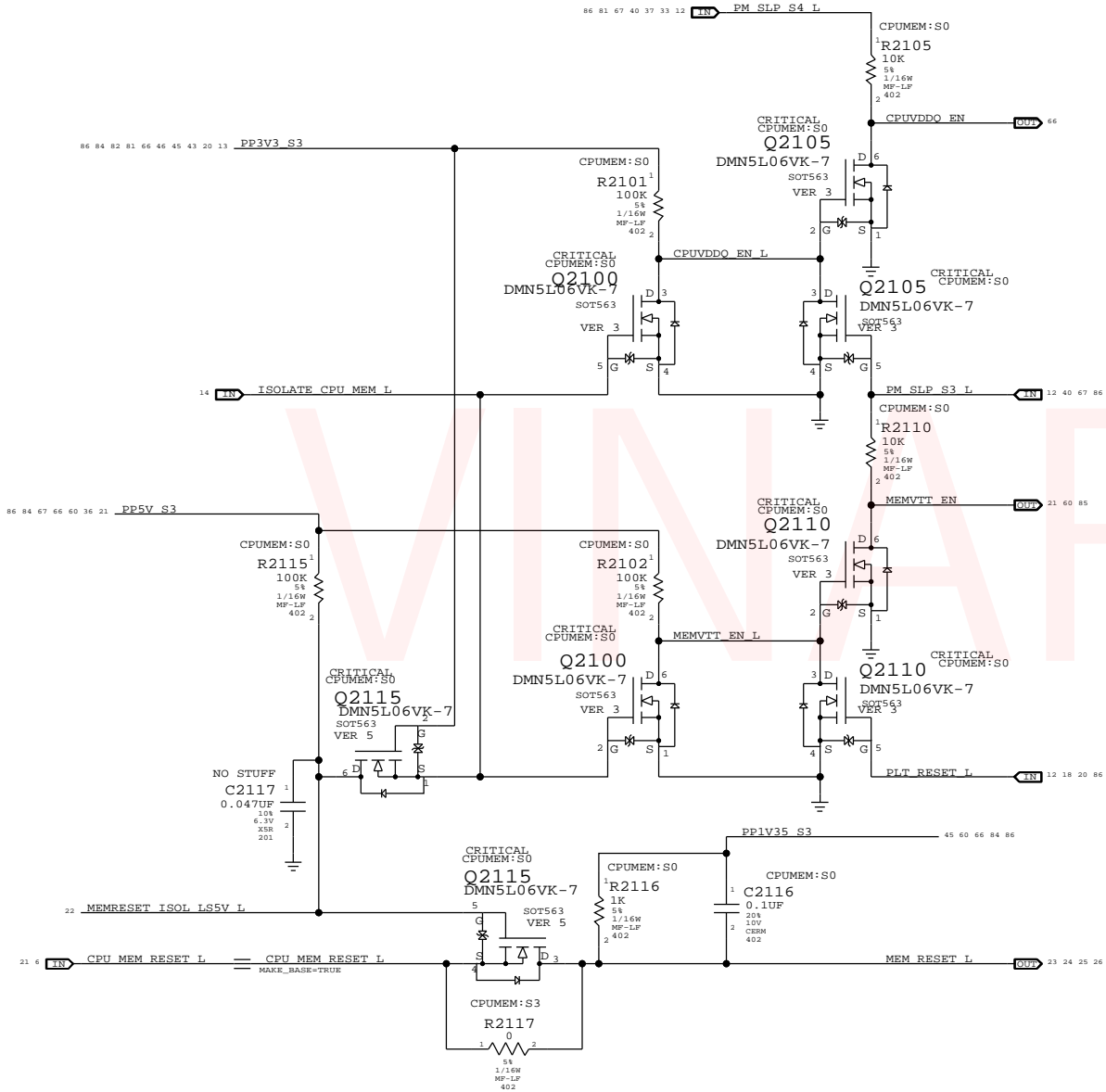
WHEN HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM\_RESET\_L not isolated.

WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM\_RESET\_L isolated.

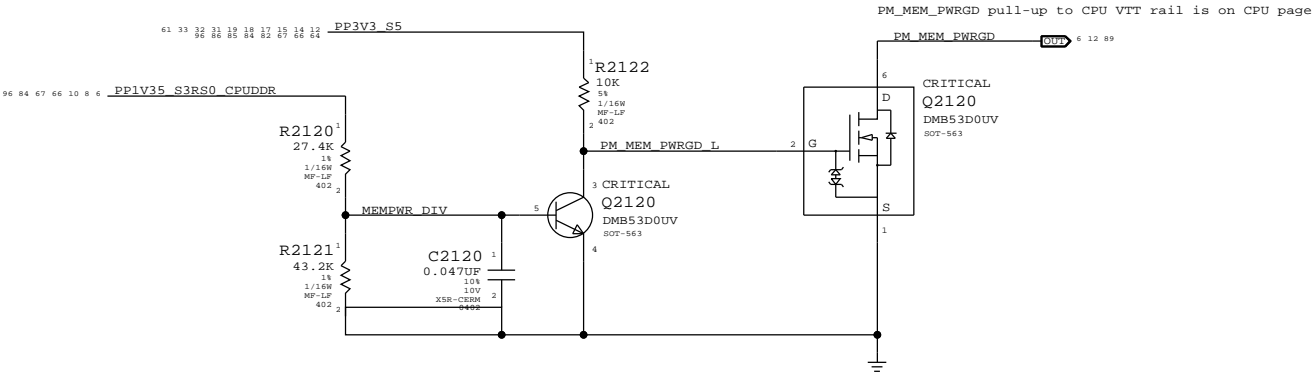
CPUVDDQ\_EN = (ISOLATE\_CPU\_MEM\_L + PM\_SLP\_S3\_L) \* PM\_SLP\_S4\_L

MEMVTT\_EN = (ISOLATE\_CPU\_MEM\_L + PLT\_RST\_L) \* PM\_SLP\_S3\_L

MEM\_RESET\_L = !ISOLATE\_CPU\_MEM\_L + CPU\_MEM\_RESET\_L

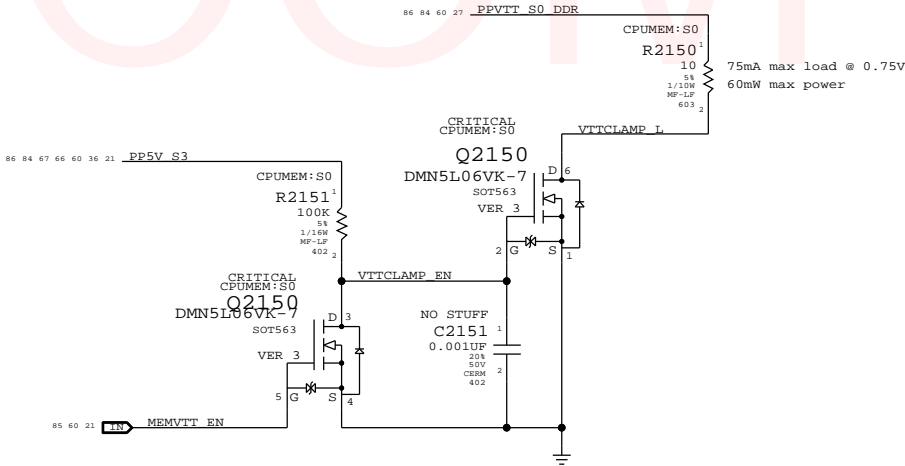


MEM S0 "PGOOD" for CPU



MEMVTT Clamp


Ensures CKE signals are held low in S3

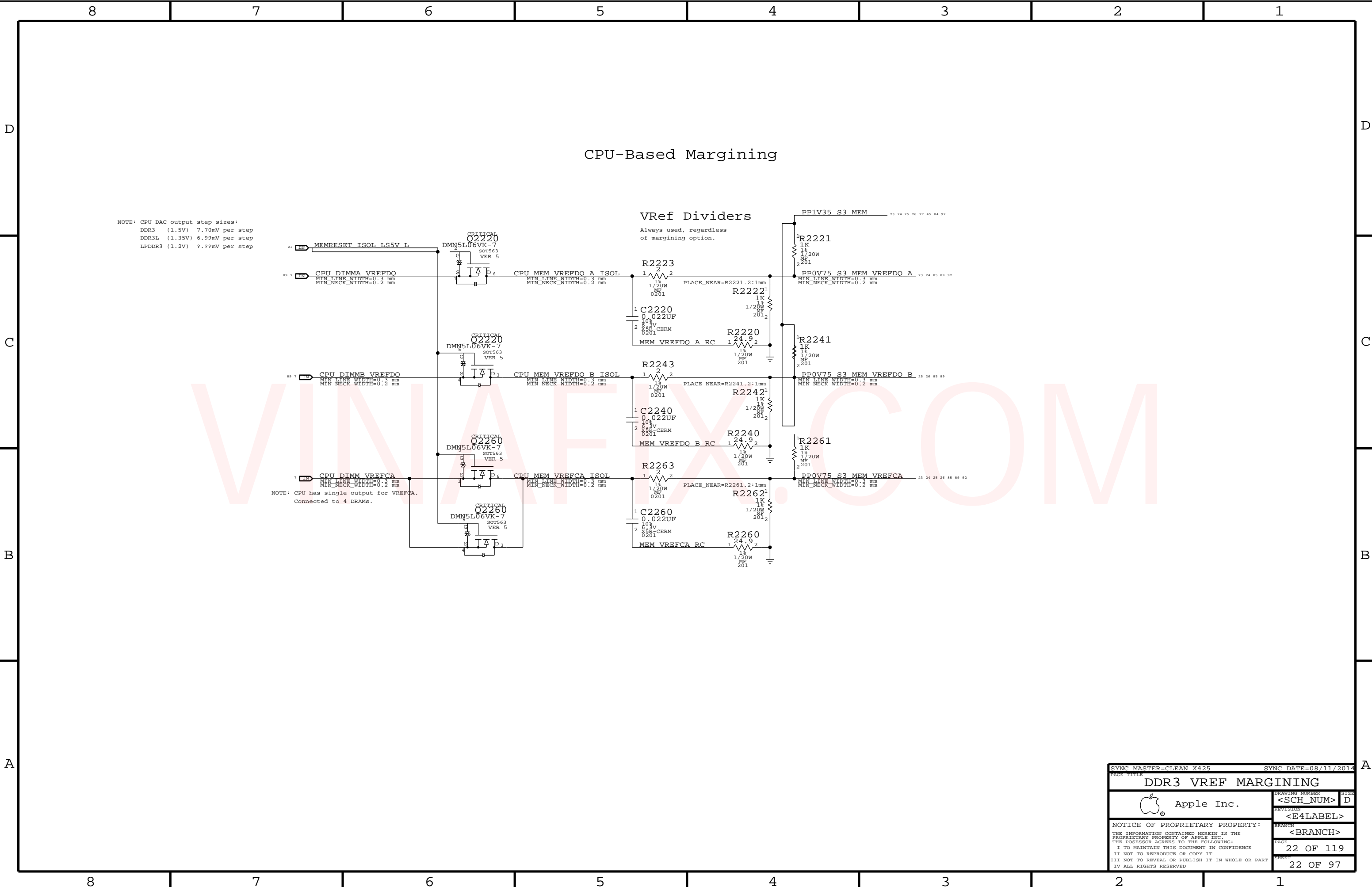


Step	SOLATE_CPU_MEM_L	PLT_RST_L	PM_SLP_S3_L	PM_SLP_S4_L	CPU_MEM_RESET_L	MEM_RESET_L	MEMVTT_EN	CPUVDDQ_EN
S0	0	1	1	1	1	CPU_MEM_RESET_L	1	1
1	1	0	1	1	1	1	1	1
2	0	0	1	1	1	1	0	1
3	0	0	0	1	X	1	0	0
4	0	0	1	1	X	1	0	1
5	0	1	1	1	0 (*)	1	1	1
6	0	1	1	1	1	1	1	1
S0	7	1	1	1	1	CPU_MEM_RESET_L	1	1

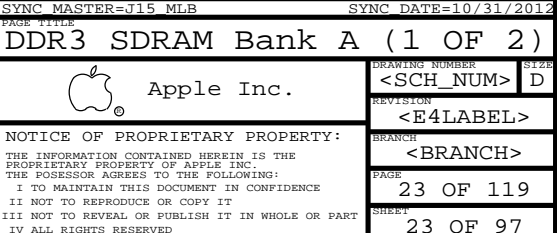
(\*) CPU\_MEM\_RESET\_L asserts due to loss of PM\_MEM\_PWRGD, must wait for software to clear before deasserting ISOLATE\_CPU\_MEM\_L GPIO.

NOTE: In the event of a S3->S5 transition ISOLATE\_CPU\_MEM\_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM\_RESET\_L will not properly assert. Software must deassert ISOLATE\_CPU\_MEM\_L and then generate a valid reset cycle on CPU\_MEM\_RESET\_L.

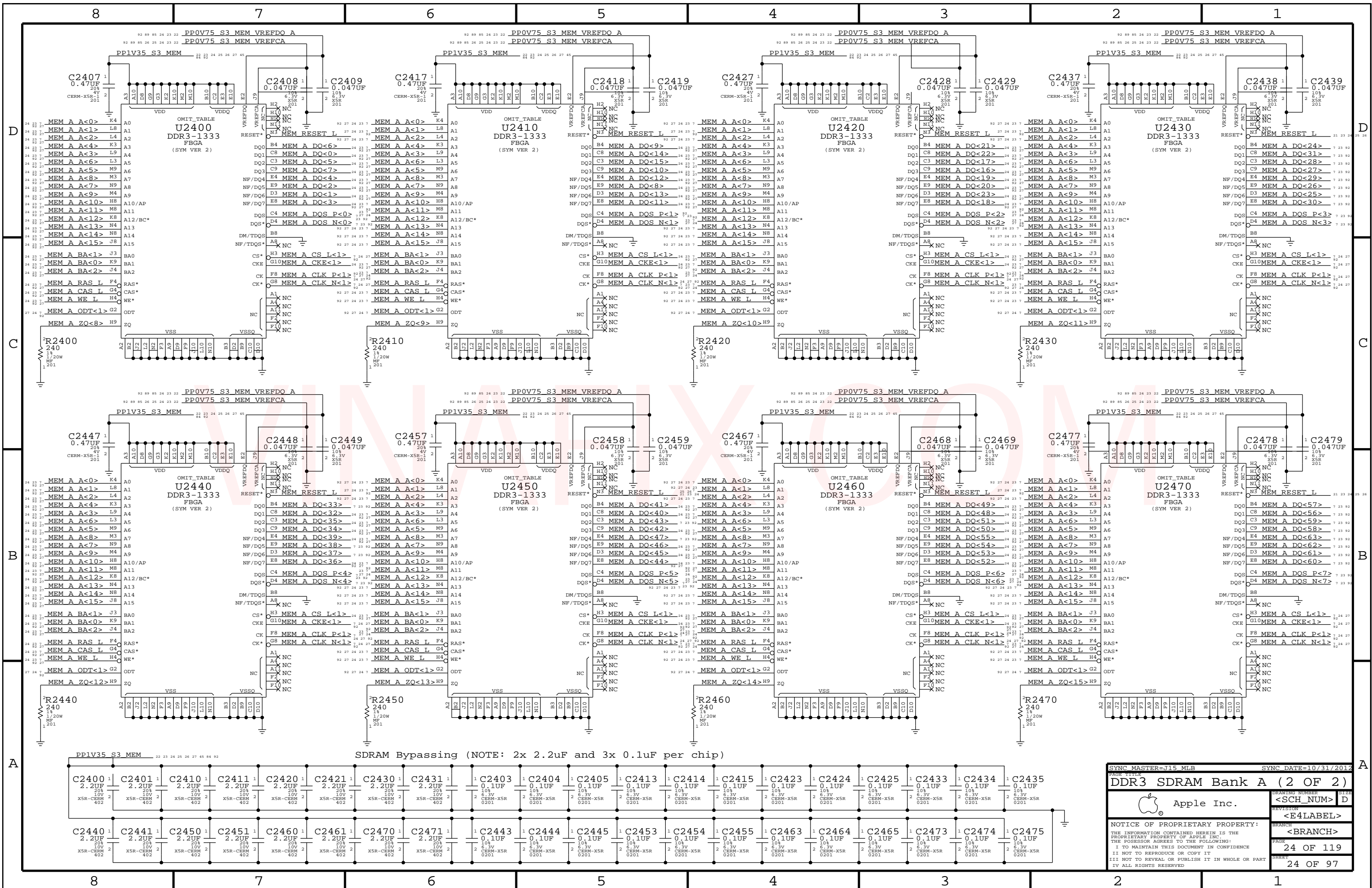
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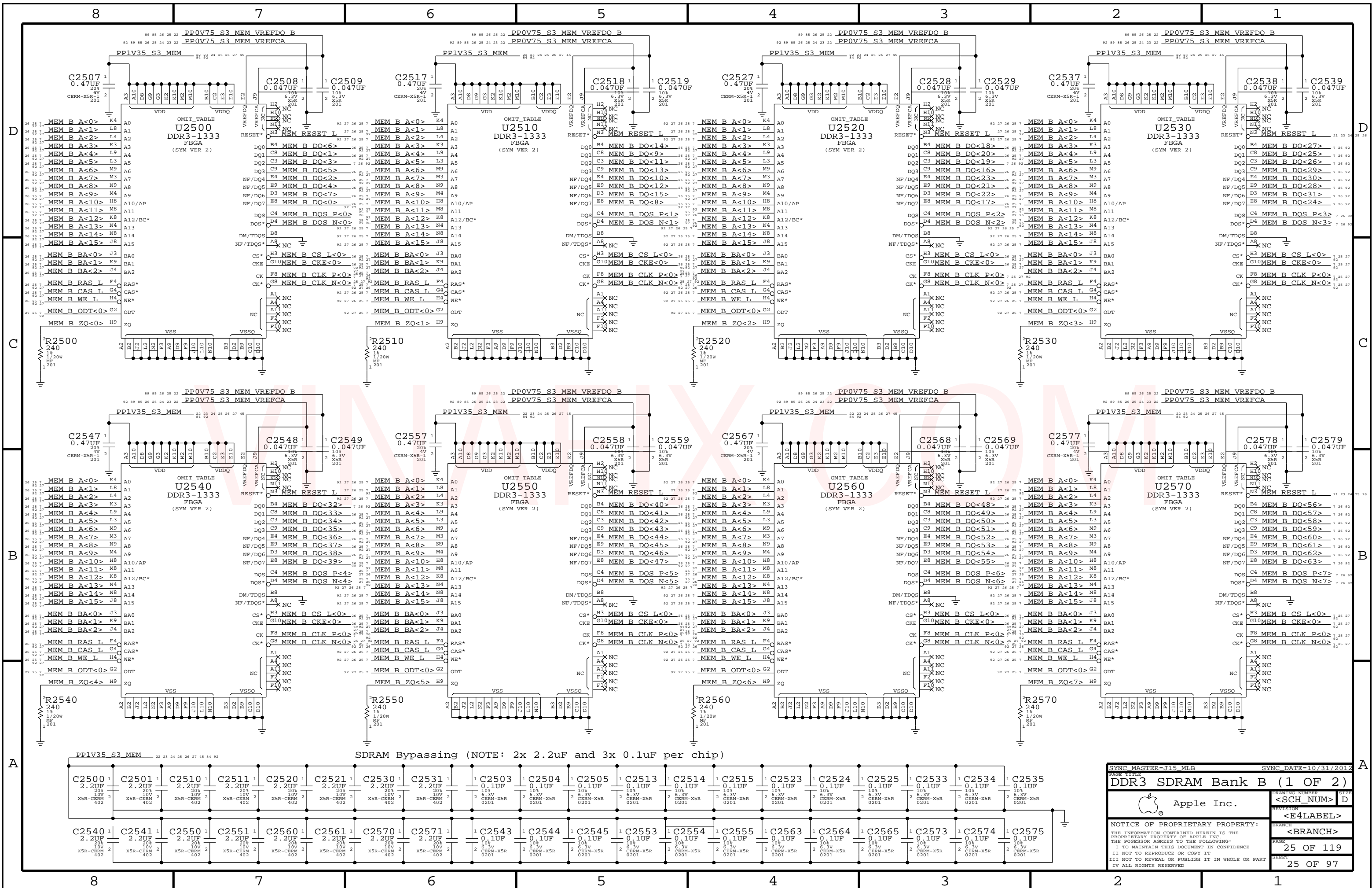






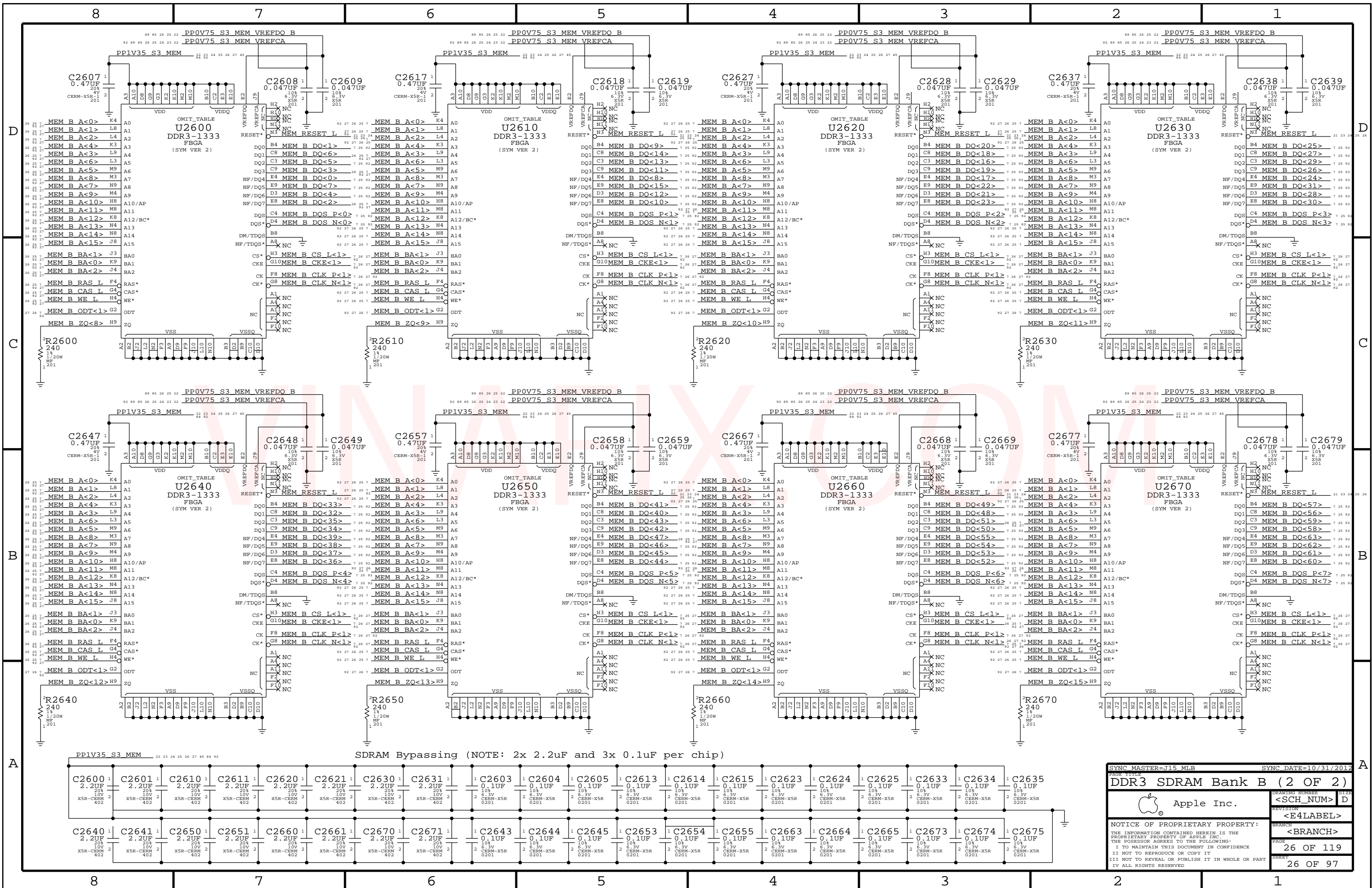
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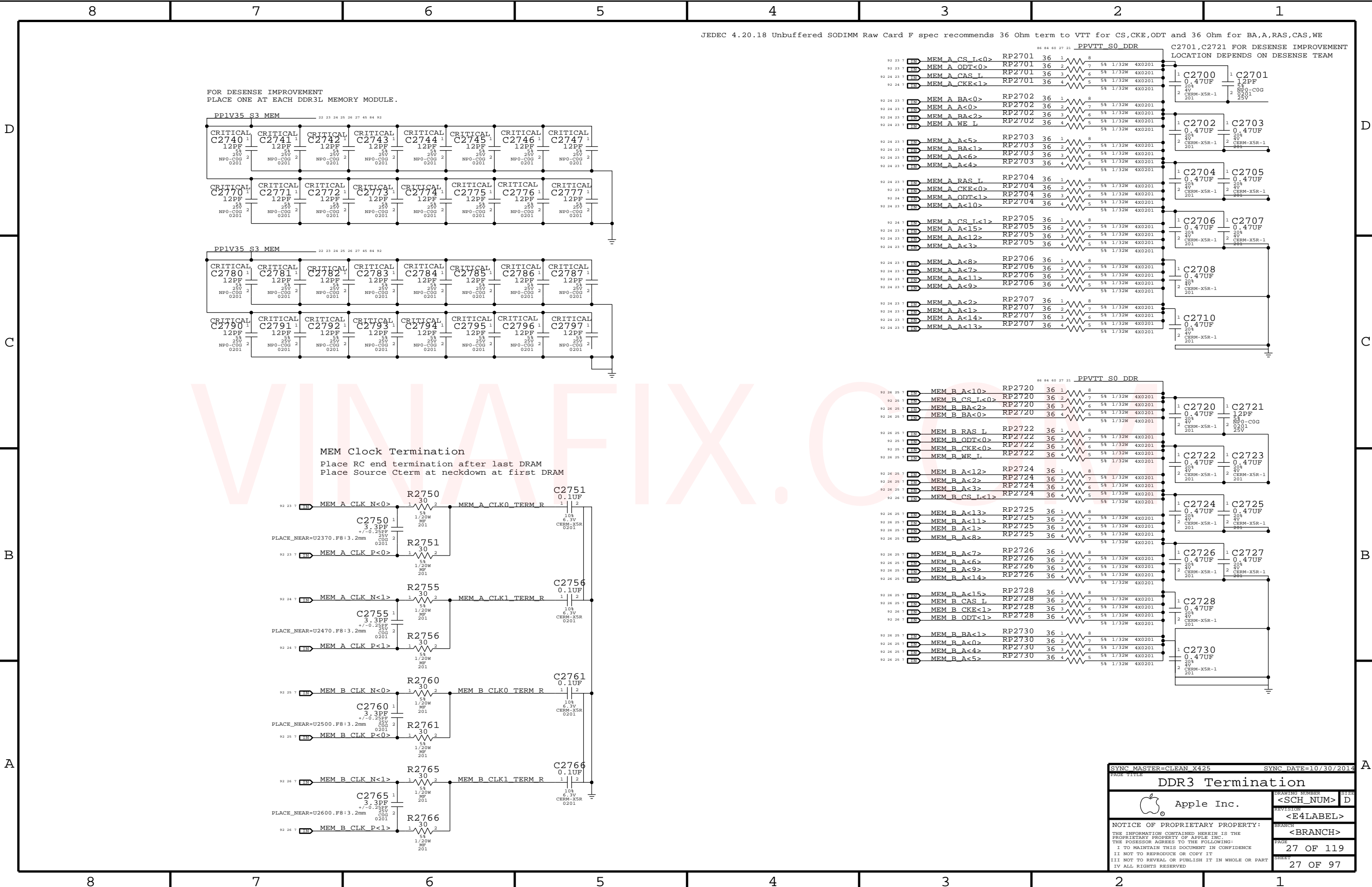


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FOR DESENSE IMPROVEMENT  
PLACE ONE AT EACH DDR3L MEMORY MODULE.

MEM Clock Termination  
Place RC end termination after last DRAM  
Place Source Cterm at neckdown at first DRAM

SYNC MASTER=CLEAN X425

SYNC DATE=10/30/2014

DDR3 Termination

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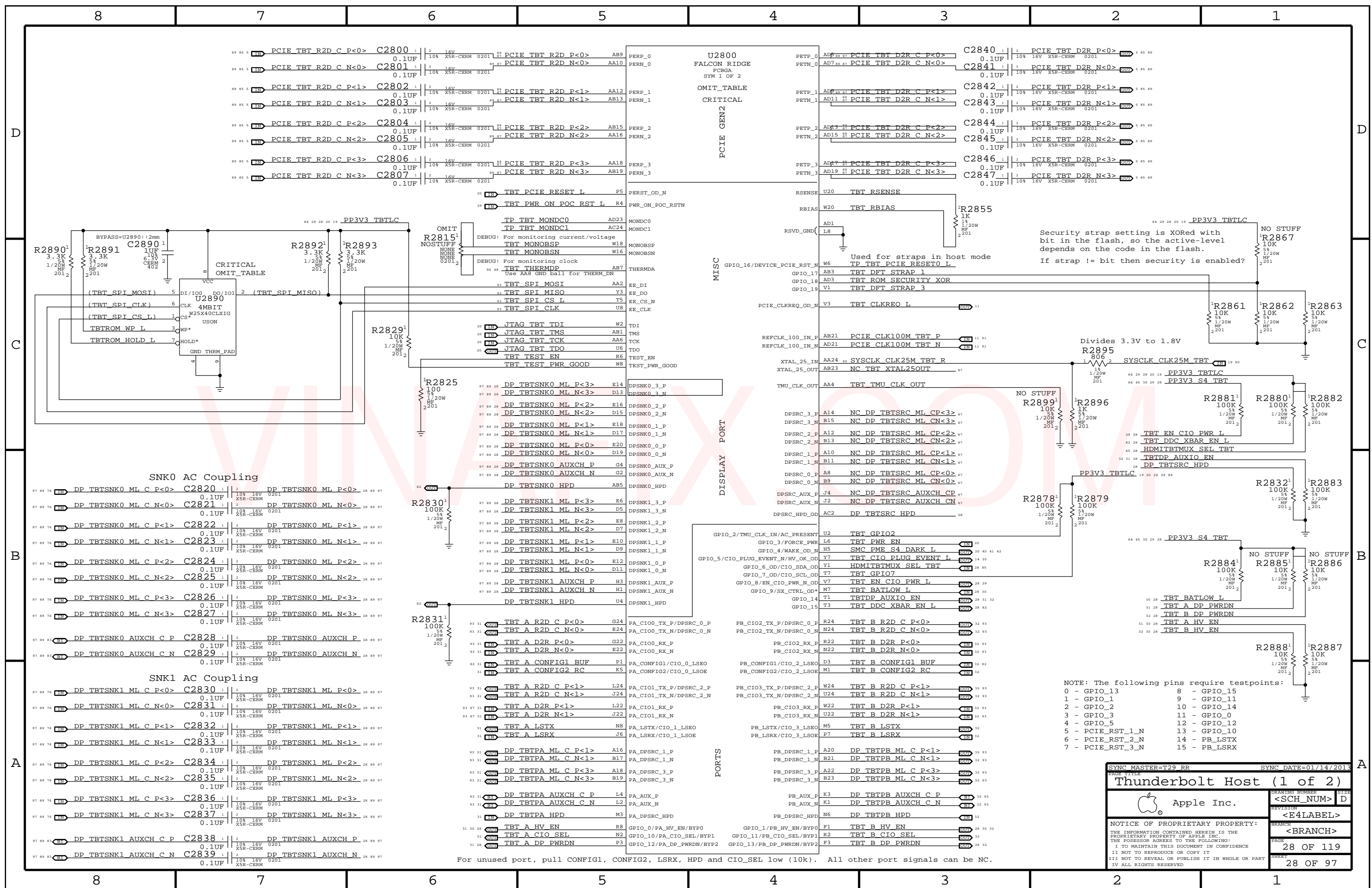
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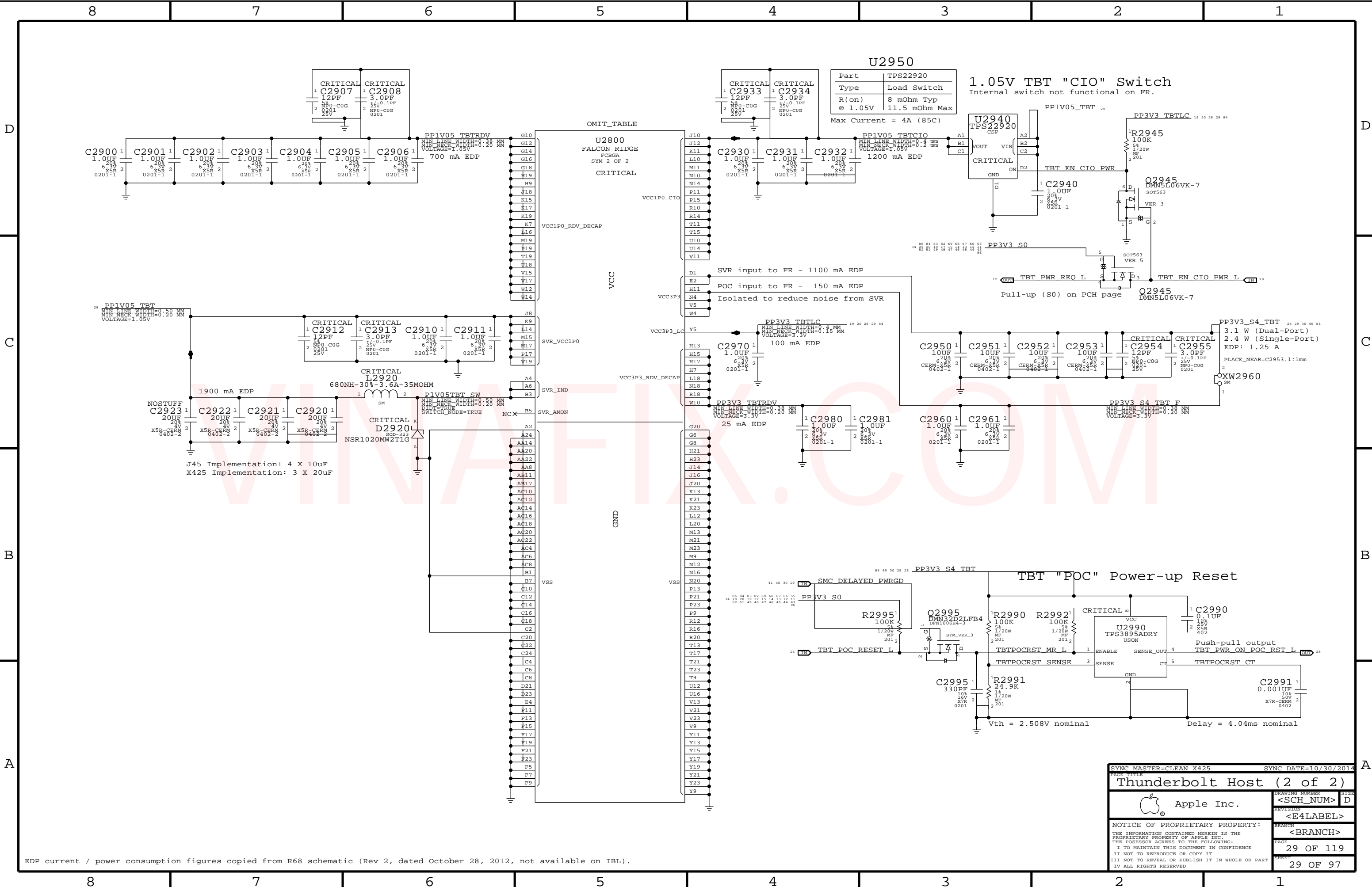
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EDP current / power consumption figures copied from R68 schematic (Rev 2, dated October 28, 2012, not available on IBL).

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Power aliases required by this page:

- =PPVIN_SW_TBTBST	(8-13V Boost Input)
- =PP15V_TBT_REG	(15V Boost Output)

---

Signal aliases required by this page:

(NONE)

---

BOM options provided by this page:

(NONE)

# Thunderbolt 15V Boost Regulator

C3080 USING 0603 PAKAGE IS FOR DFM TO PROTECT Q3080 (CSP)

CRITICAL

SI8409DB: Vds(max): -30V  
Vgs(max): +/-12V  
Vgs(th): -1.4V  
Rds(on): 46mOhm @ 4.5V Vgs  
Id(max): 3.7A @ 70C

Q3080 SI8409DB BGA

PPBUS G3H 8-13V Input Changes required for 2S.

R3080 470K 10% 1/16W MF-LF 402

C3080 0.1UF 25V 603-1

TBTBST PWREN DIV L

R3081 330K 10% 1/16W MF-LF 402

TBTBST PWREN L

Q3005 DMN5L06VK-7 SOT563

VER 3

TBT A HV EN

Q3005 DMN5L06VK-7 SOT563

VER 3

TBT B HV EN

R3092 73.2K 1% 1/16W MF-LF 402

C3085 2.2UF 20% 10V CER-X6S 0402

C3086 2.2UF 20% 10V CER-X6S 0402

C3087 68PF 50V 50V CERM 0402

R3093 49.9K 1% 1/16W MF-LF 402

TBTBST VC RC

C3092 2.2UF 20% 10V CER-X6S 0402

C3093 0.0033UF 10% 50V X7R-CERM 0402

R3094 26.7K 1% 1/16W MF-LF 402

C3094 0.33UF 10% 25V X5R-CERM 0402

GND TBTBST SGND

Q3088 DMN5L06VK-7 SOT563

VER 3

Max Vgs: 10V

TBTBST SHDN DIV

R3087 330K 10% 1/16W MF-LF 402

Q3088 DMN5L06VK-7 SOT563

VER 3

SMC DELAYED PWRGD

CRITICAL

L3095 3.3UH-6.5A PIMB063T-SM

TBTBST BOOST

U3090 LT3957 QFN

EN/UVLO

INTVCC

VC

RT

SS

SYNC

SGND

GND

FBX

NC

R3089 100PF 50V 50V CERM 402

C3088 10PF 50V 50V CERM 0402

R3095 137K 1% 1/16W MF-LF 402

R3096 15.8K 1% 1/16W MF-LF 402

R3097 10K 1% 1/16W MF-LF 402

C3095 33UF-0.060OHM 25V 25V POLY-TANT CASE-D3L

C3096 10UF 20% 25V X5R-CERM 0603

C3097 10UF 10% 25V X7R-CERM 1206

C3098 10UF 10% 25V X5R-CERM 0603

C3099 0.001UF 10% 50V X7R-CERM 0402

R3089 100PF 50V 50V CERM 402

R3095 137K 1% 1/16W MF-LF 402

R3096 15.8K 1% 1/16W MF-LF 402

R3097 10K 1% 1/16W MF-LF 402

C3095 33UF-0.060OHM 25V 25V POLY-TANT CASE-D3L

C3096 10UF 20% 25V X5R-CERM 0603

C3097 10UF 10% 25V X7R-CERM 1206

C3098 10UF 10% 25V X5R-CERM 0603

C3099 0.001UF 10% 50V X7R-CERM 0402

D3095 PDS540XF PWRD15

NOTE: Change R3097 to XW3095 at PVT

Vout = 15.47V  
Max Current = 2A?  
Freq = 480KHz


Vout = 1.6V \* (1 + Ra / Rb)

NOTE: MIRROR C3096 and C3098

PLACE\_SIDE=TOP

PLACE\_SIDE=BOTTOM

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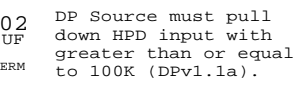
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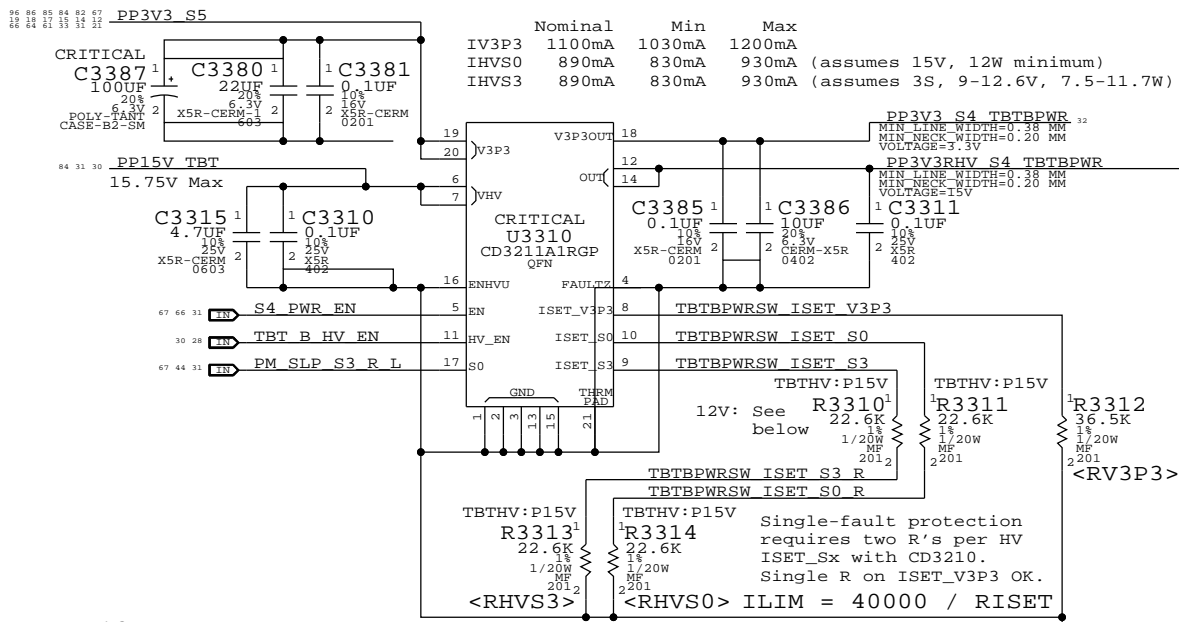
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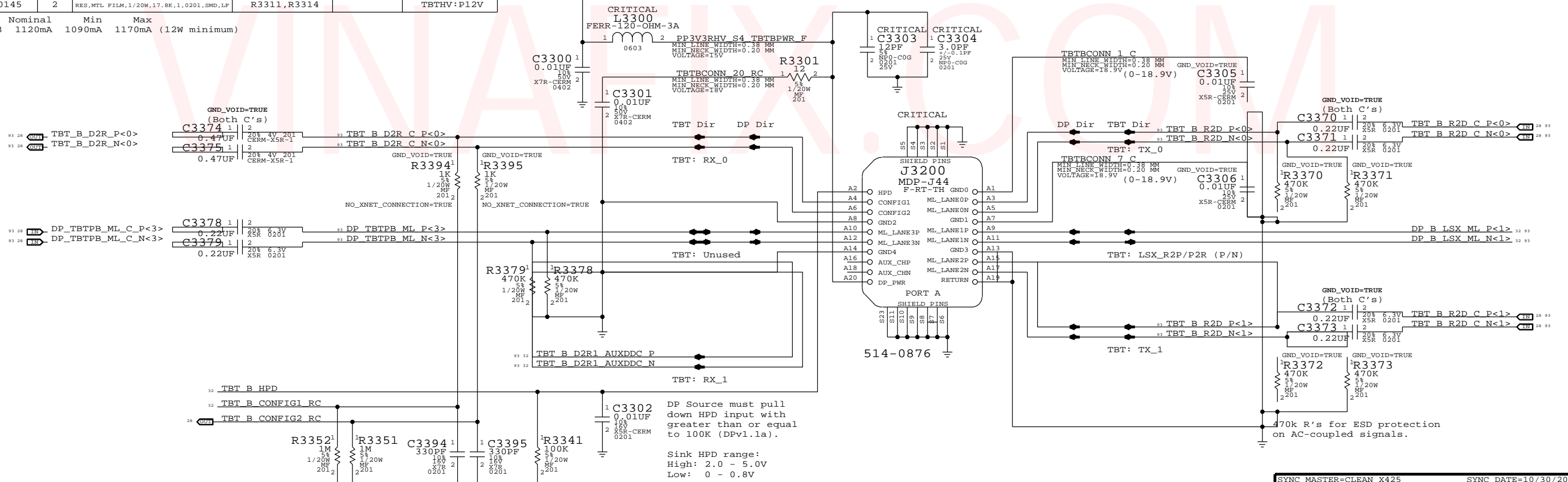
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### 3.3V/HV Power MUX

V3P3 must be S4 to support wake from Thunderbolt devices.



### Thunderbolt Connector B



SYNC MASTER=CLEAN X425		SYNC DATE=10/30/2014	
Thunderbolt Connector B			
Apple Inc.		DRAWING NUMBER	SIZE
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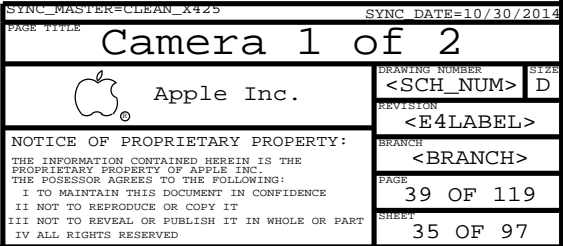
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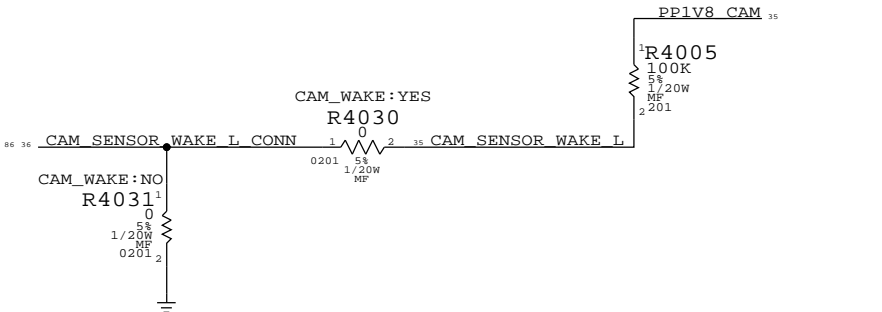
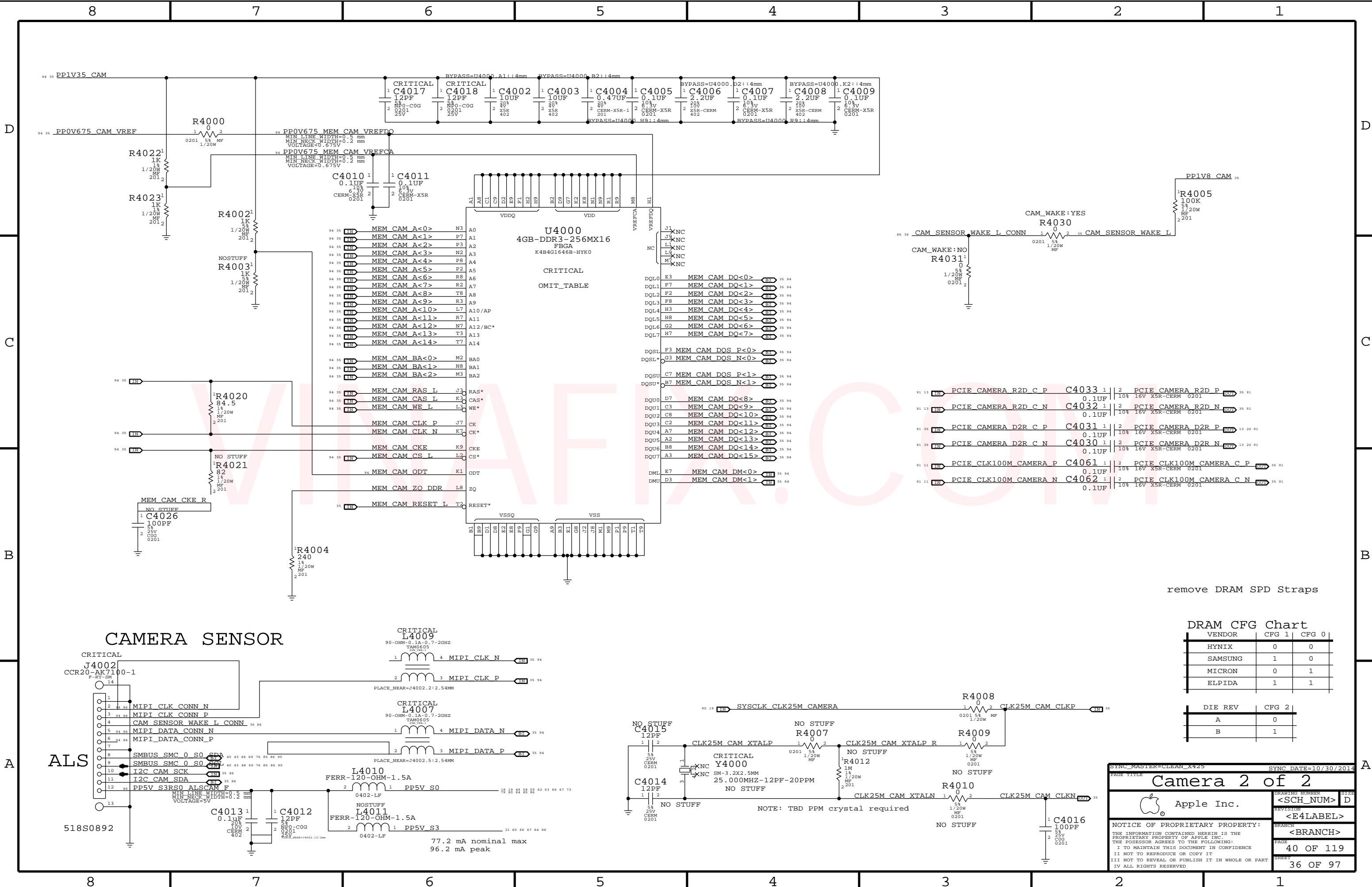












PCIE CAMERA R2D C P	C4033	1	2	PCIE CAMERA R2D P	35	91
PCIE CAMERA R2D C N	C4032	1	2	PCIE CAMERA R2D N	35	91
PCIE CAMERA D2R C P	C4031	1	2	PCIE CAMERA D2R P	13	20
PCIE CAMERA D2R C N	C4030	1	2	PCIE CAMERA D2R N	13	20
PCIE CLK100M CAMERA P	C4061	1	2	PCIE CLK100M CAMERA C P	35	91
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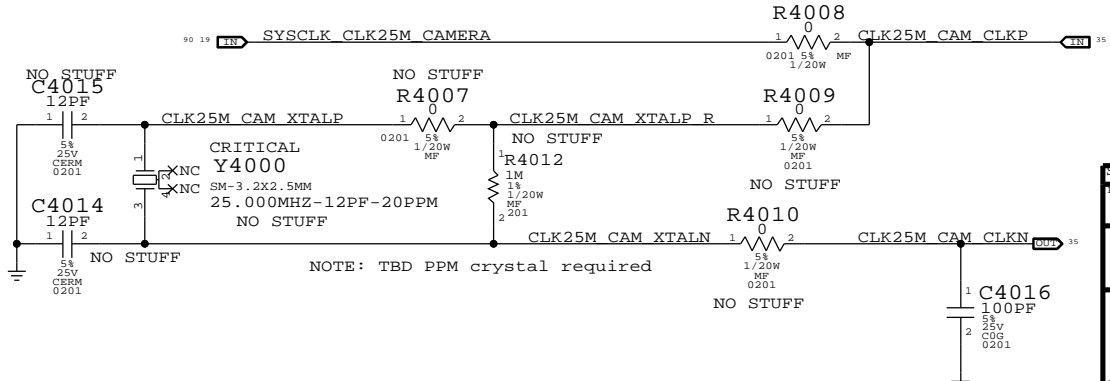
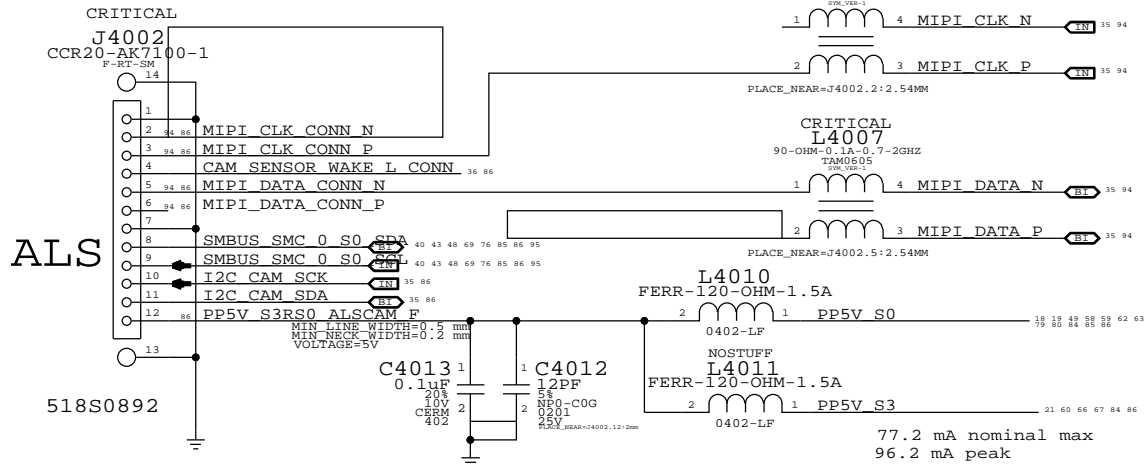
remove DRAM SPD Straps

DRAM CFG Chart

VENDOR	CFG 1	CFG 0
HYNIX	0	0
SAMSUNG	1	0
MICRON	0	1
ELPIDA	1	1

DIE REV	CFG 2
A	0
B	1

CAMERA SENSOR



Camera 2 of 2

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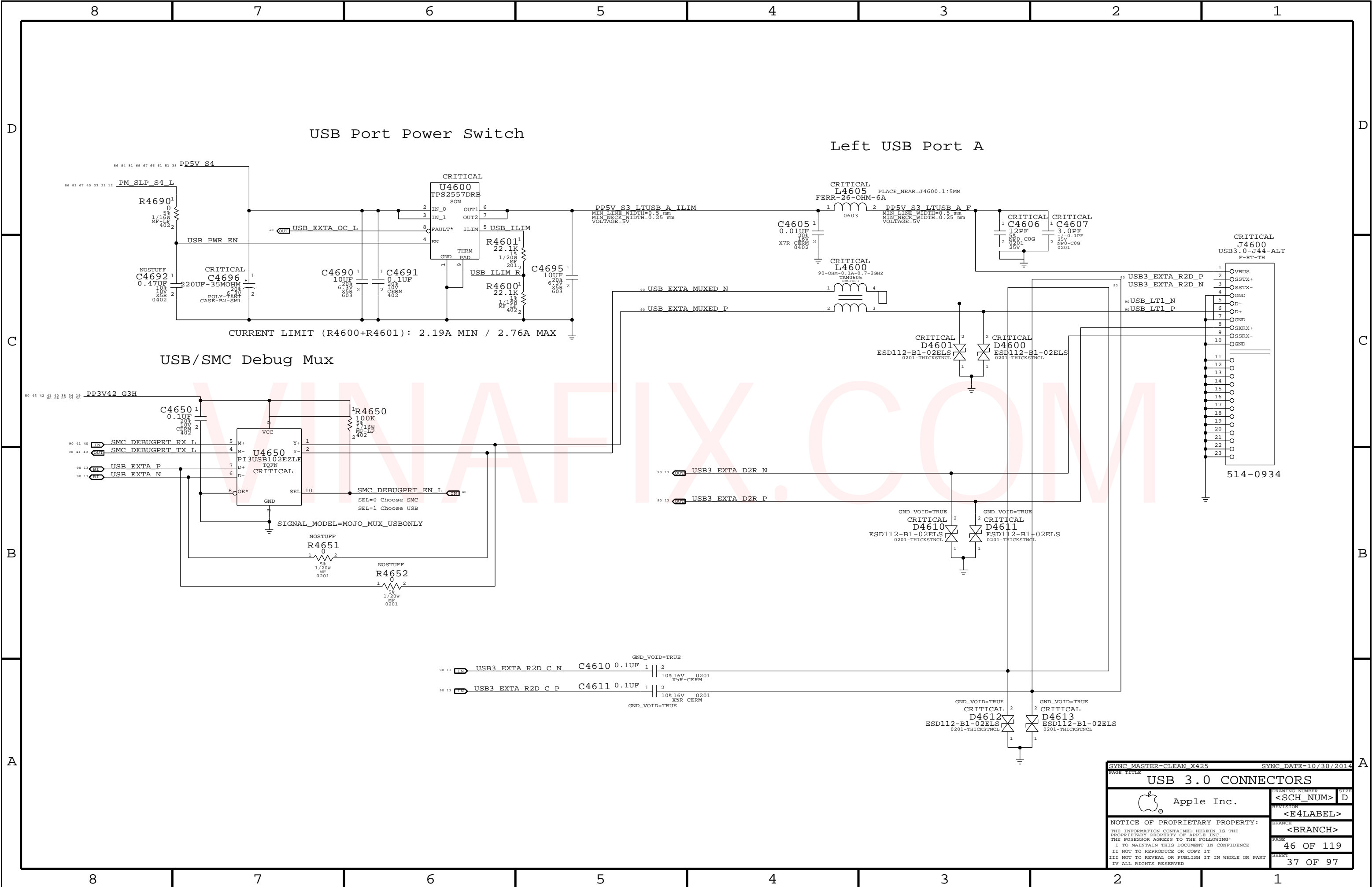
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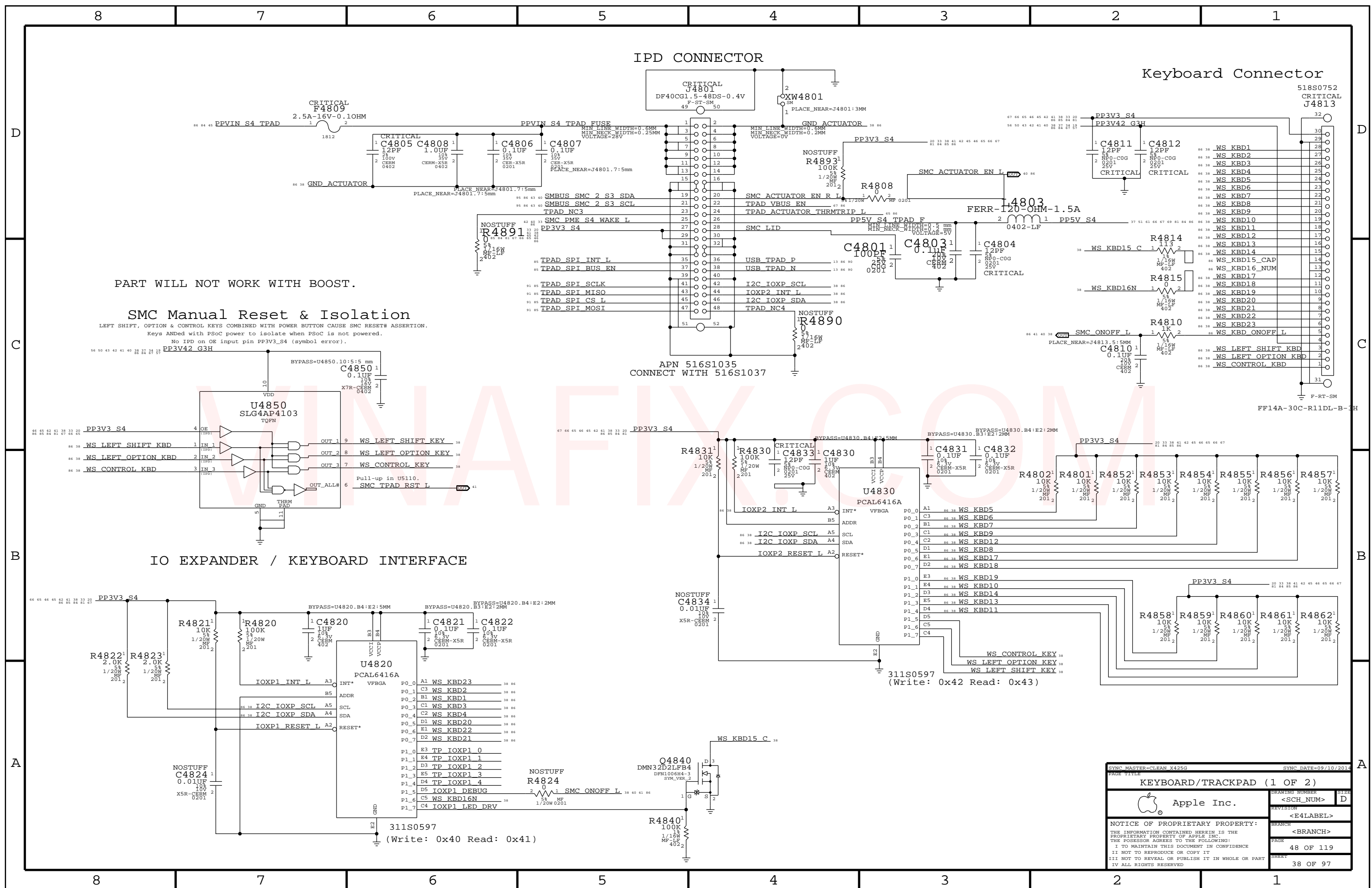
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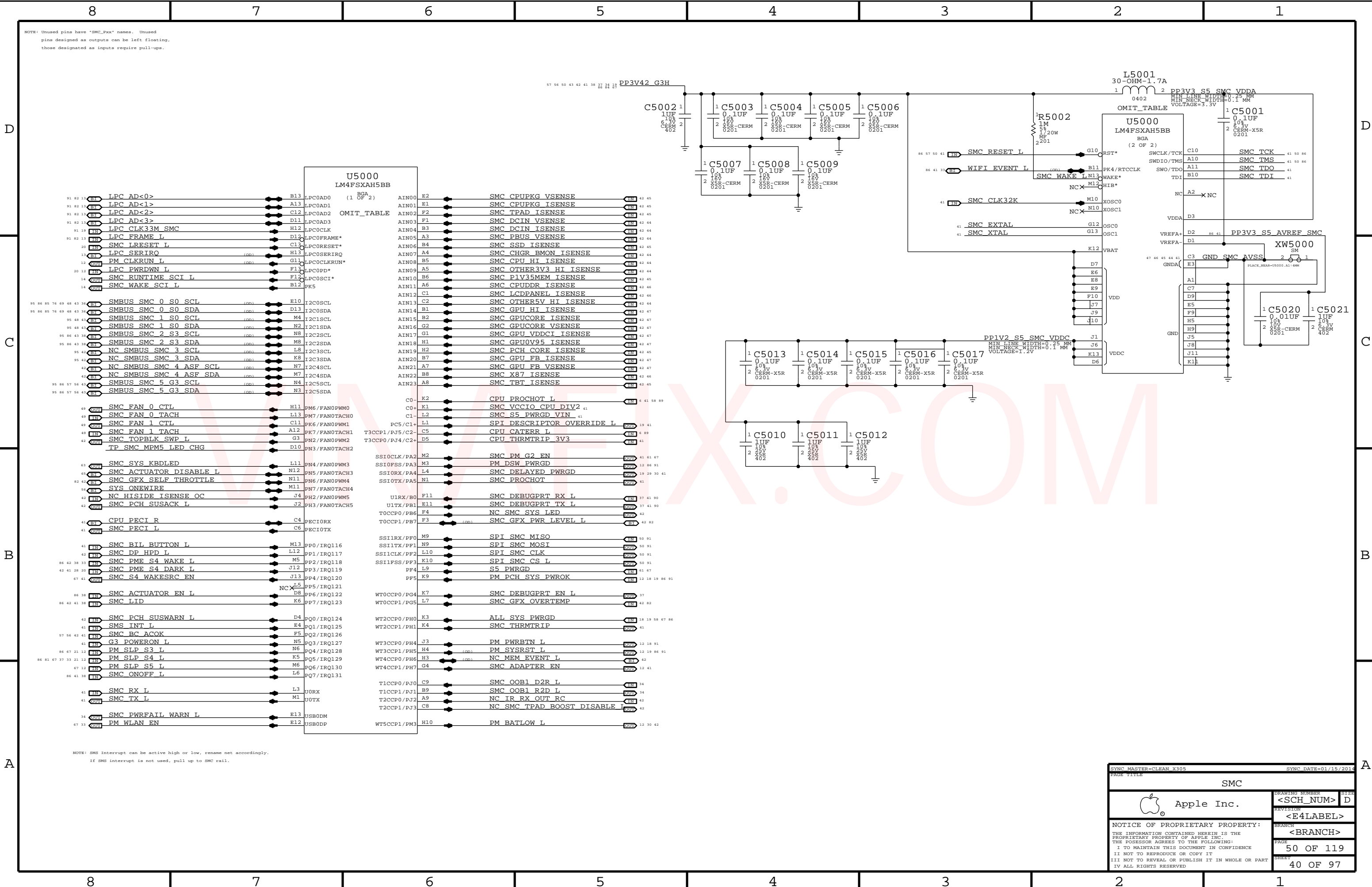
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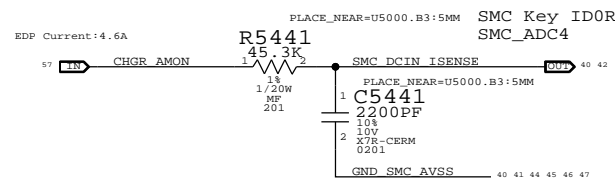
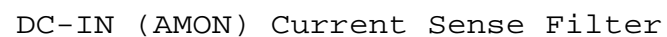
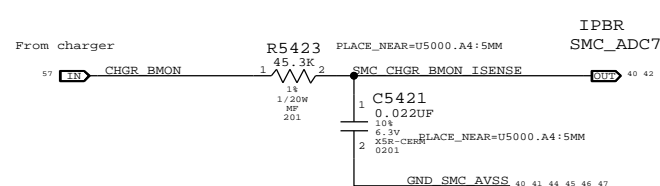
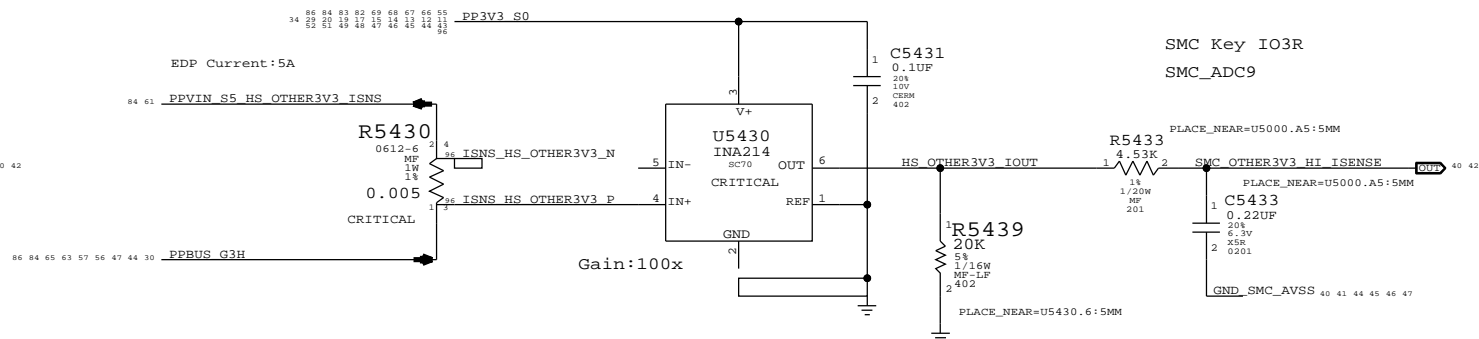
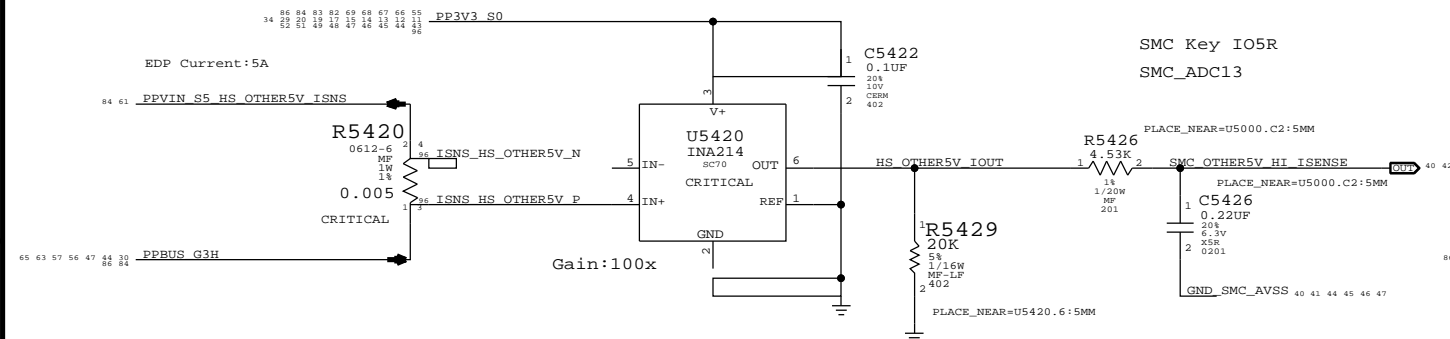
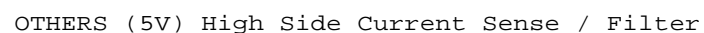
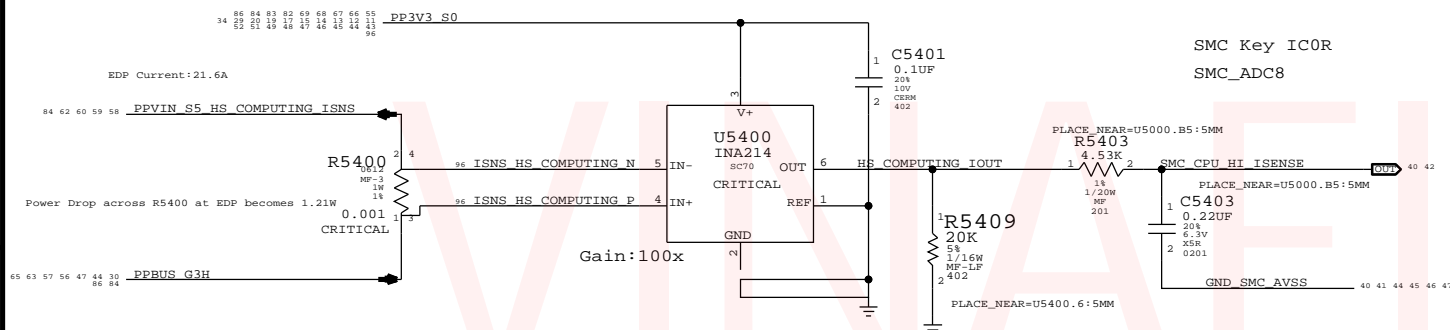
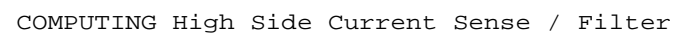
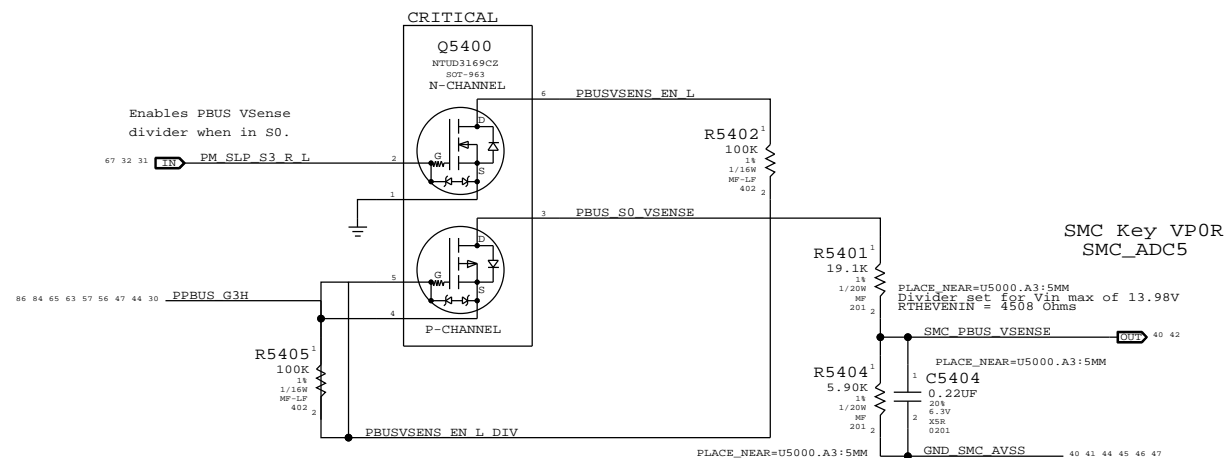
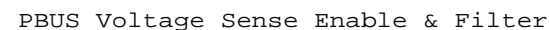
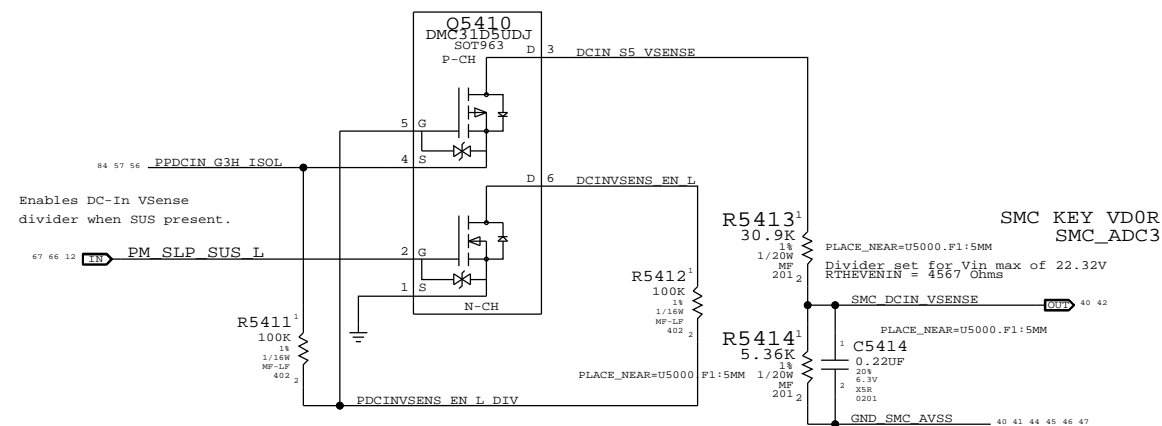







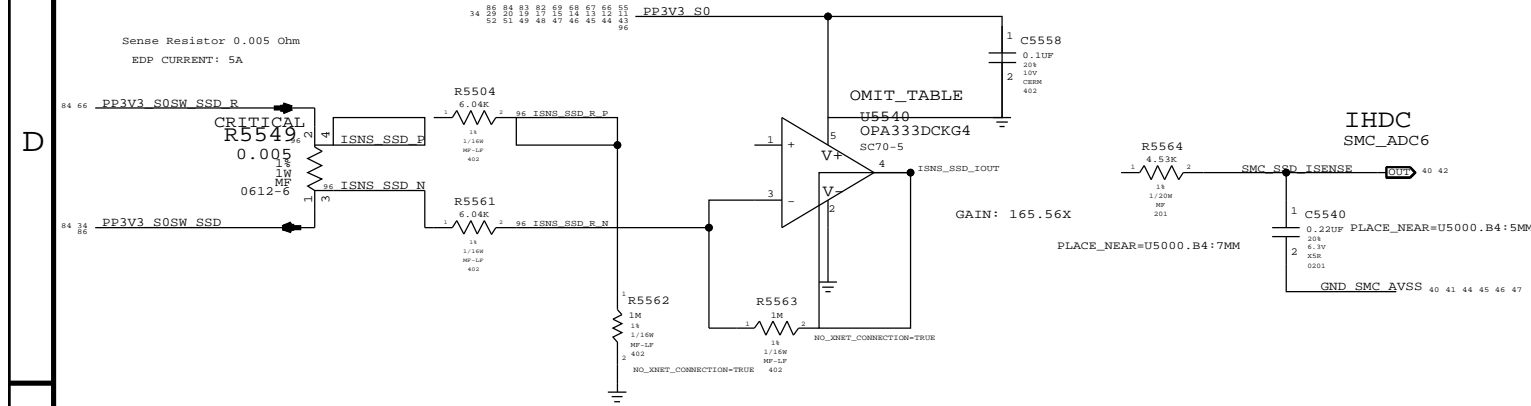




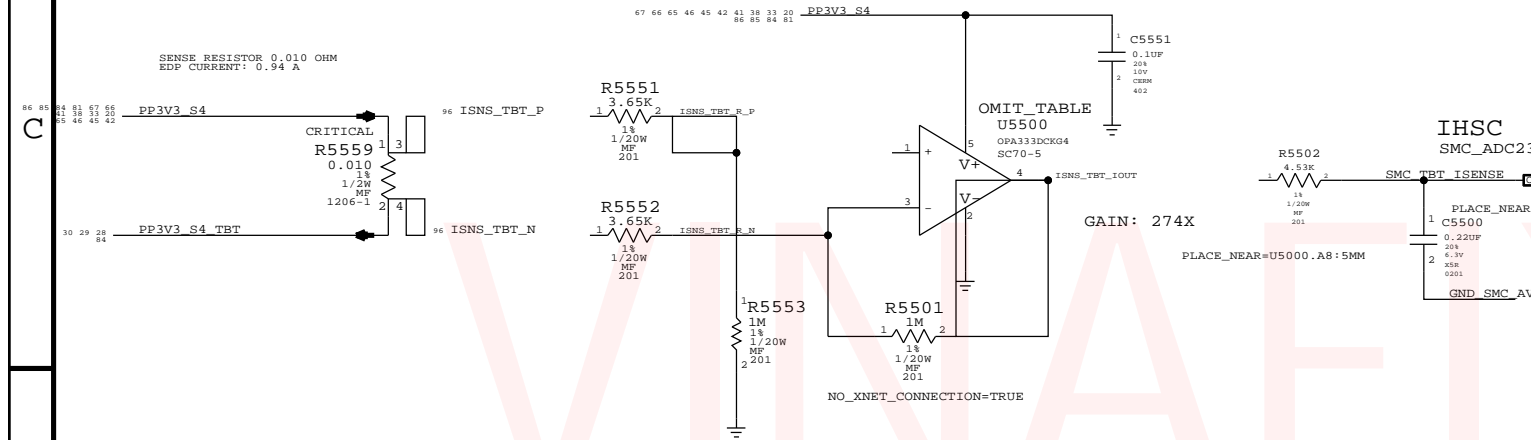


SYNC MASTER-CLEAN X305 PEG		SYNC DATE=02/18/2014	
PART TITLE			
High Side Voltage and Current Sensing			
 Apple Inc.		DRAWING NUMBER <b>&lt;SCH_NUM&gt;</b>	
		SIZE <b>D</b>	
		REVISION <b>&lt;E4LABEL&gt;</b>	
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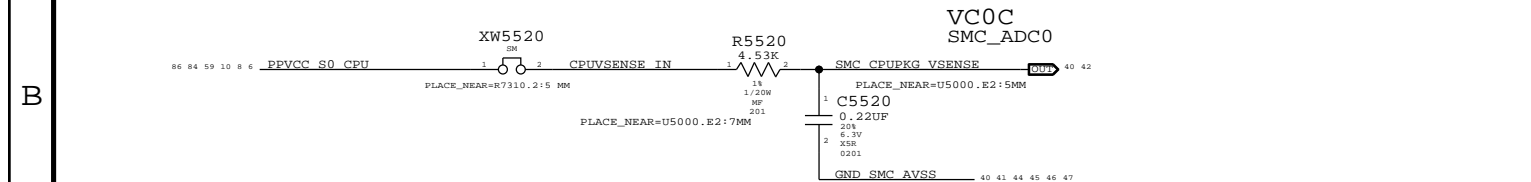
# SSD CURRENT SENSE



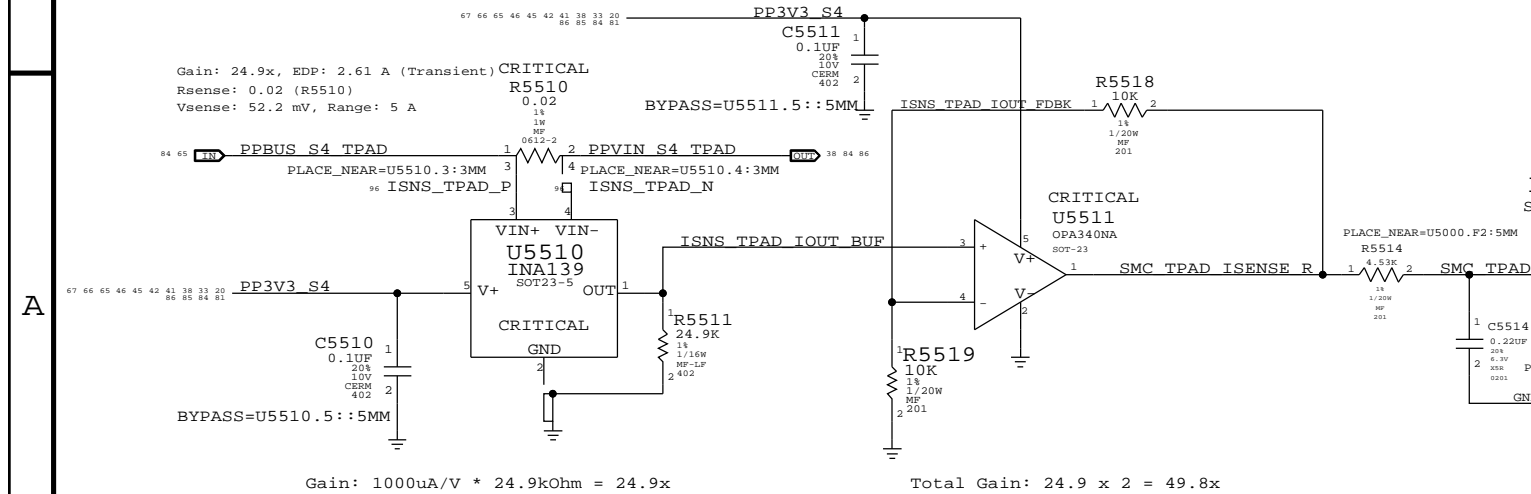
# TBT Router CURRENT SENSE



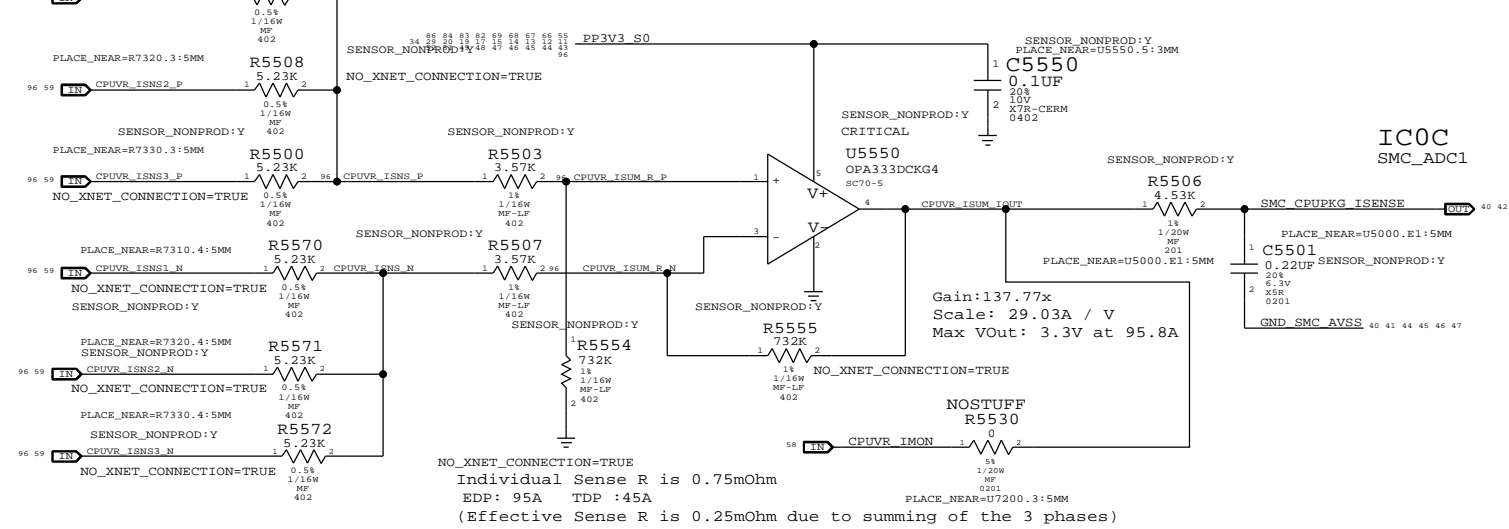
# CPU Vcore Voltage Sense / Filter



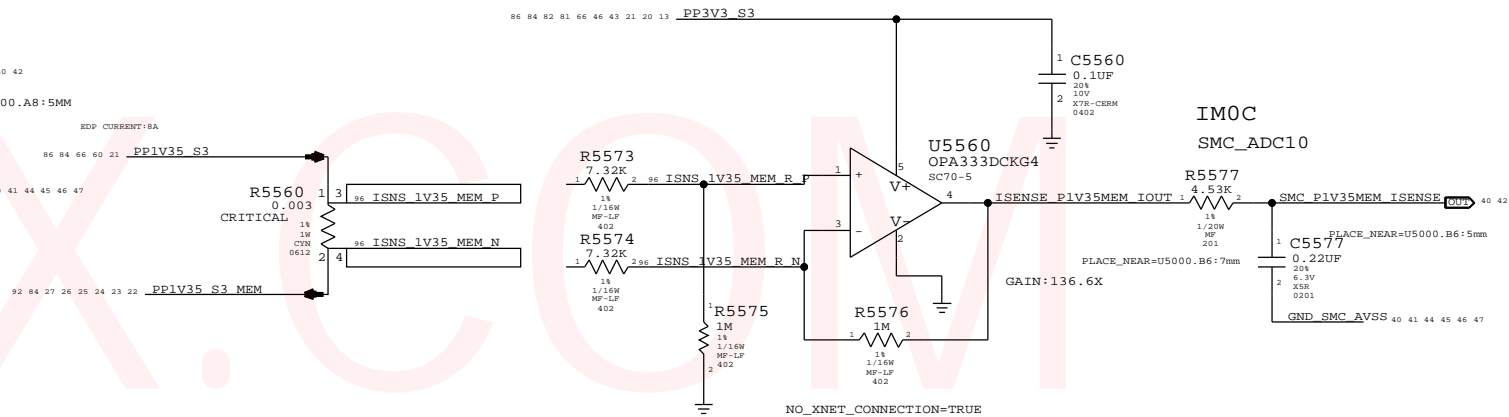
# TRACKPAD CURRENT SENSE



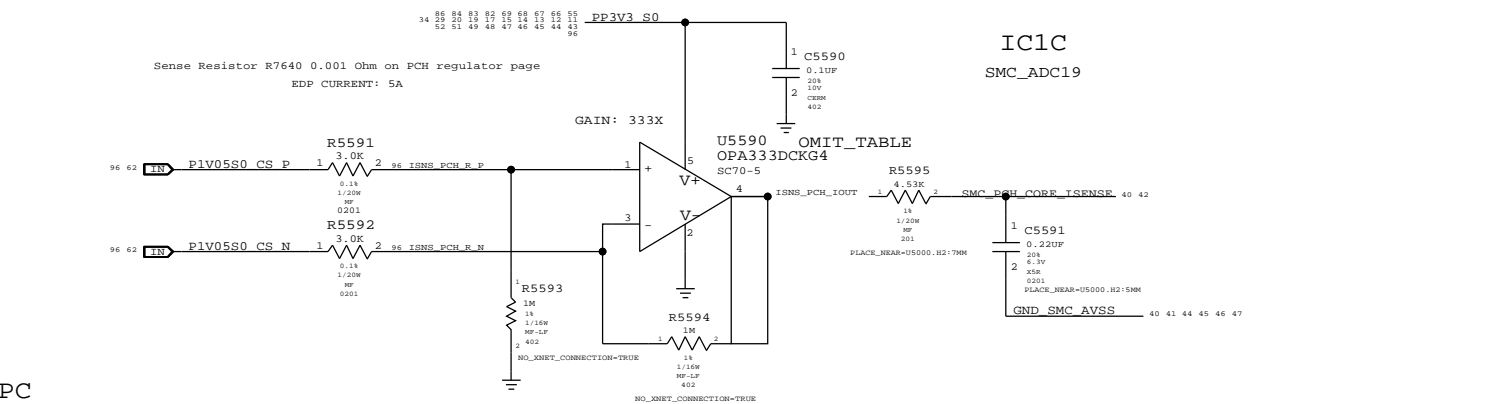
# CPU PKG Load Side Current Sense / Filter



# DDR3L 1.35V DRAM ONLY CURRENT SENSE / FILTER



# PCH CORE CURRENT SENSE



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S00107	3	IC, OPAMP, NCS333Q3, SC70-5	U5500, U5540, U5590	CRITICAL	

SYNC MASTER=CLEAN X425G

SYNC DATE=09/10/2014

Load Side Voltage and Current Sensing

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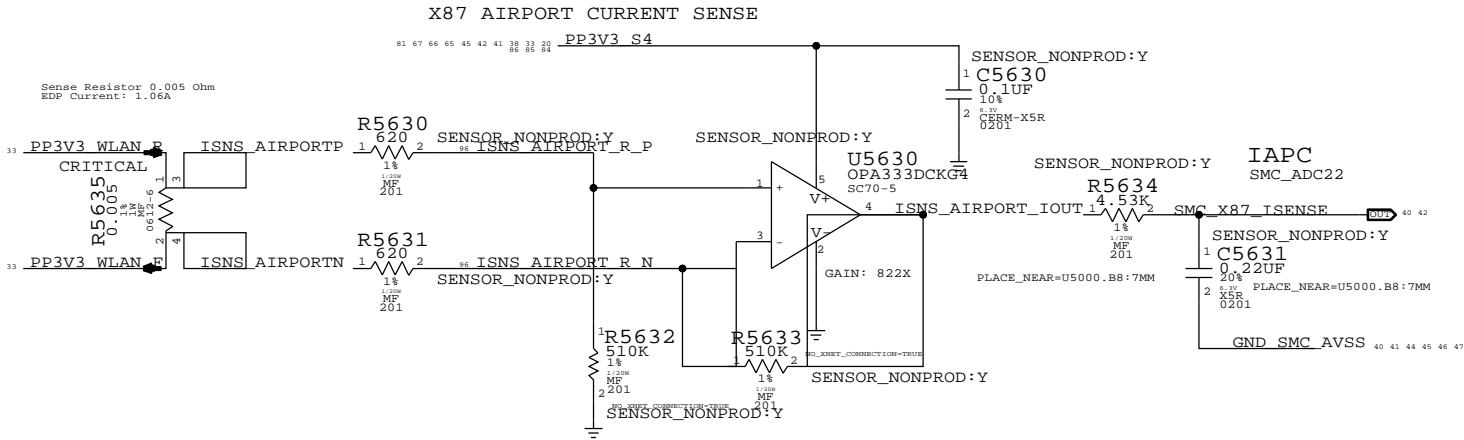
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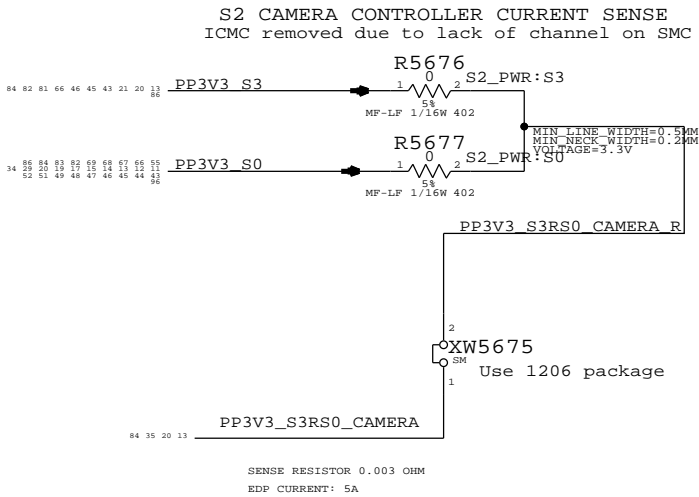
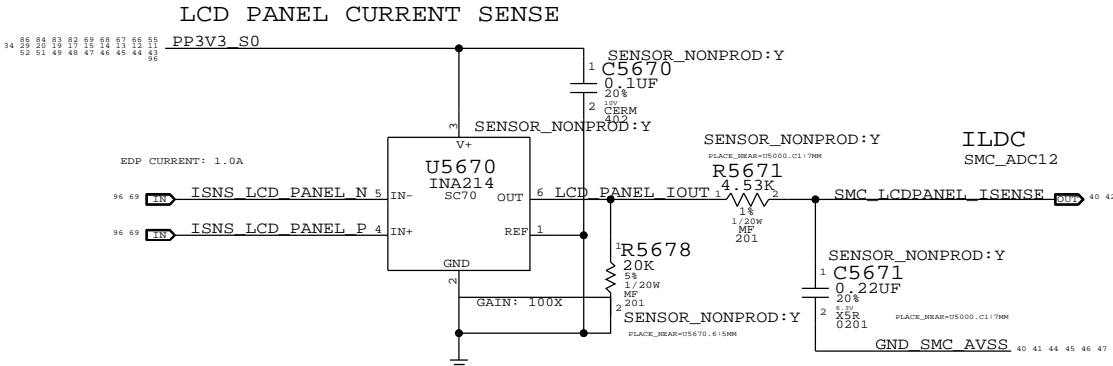
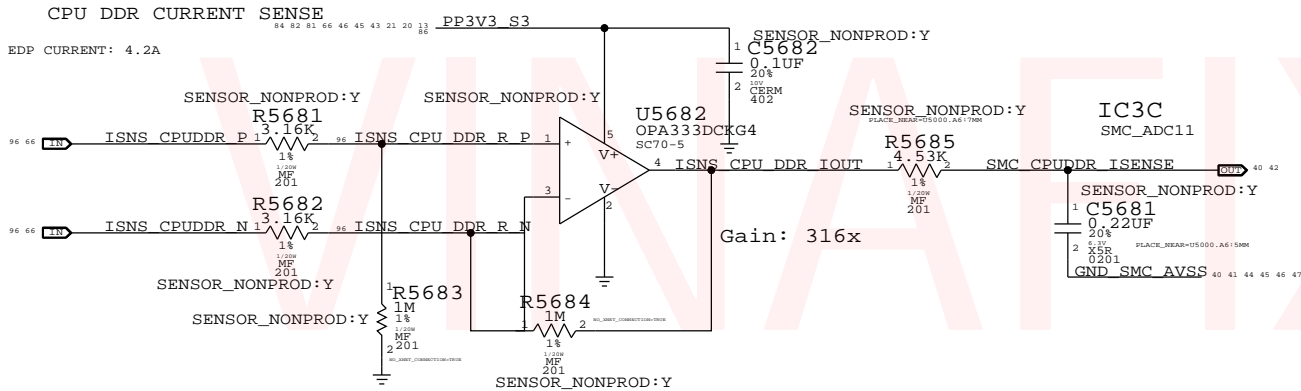
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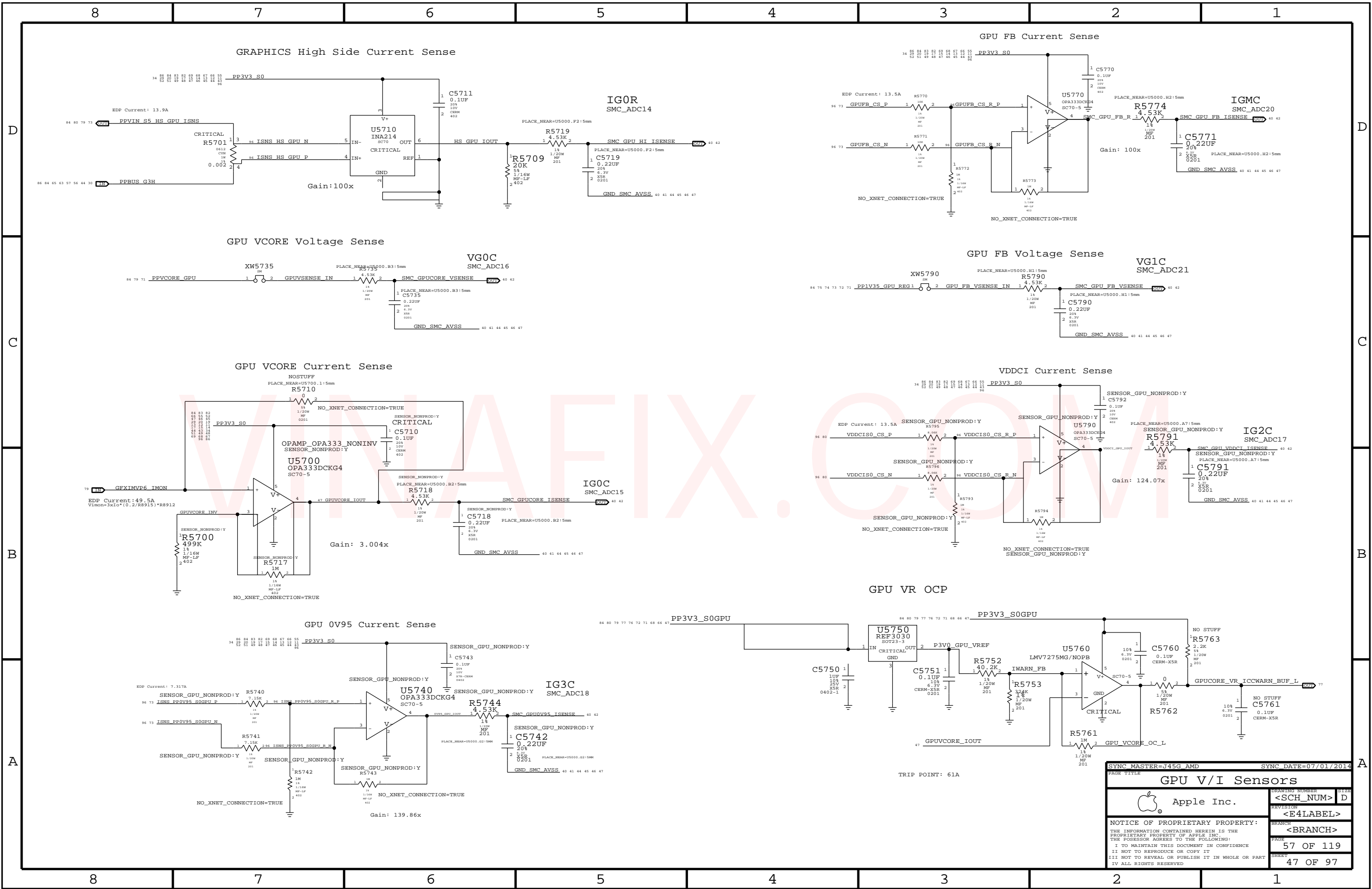


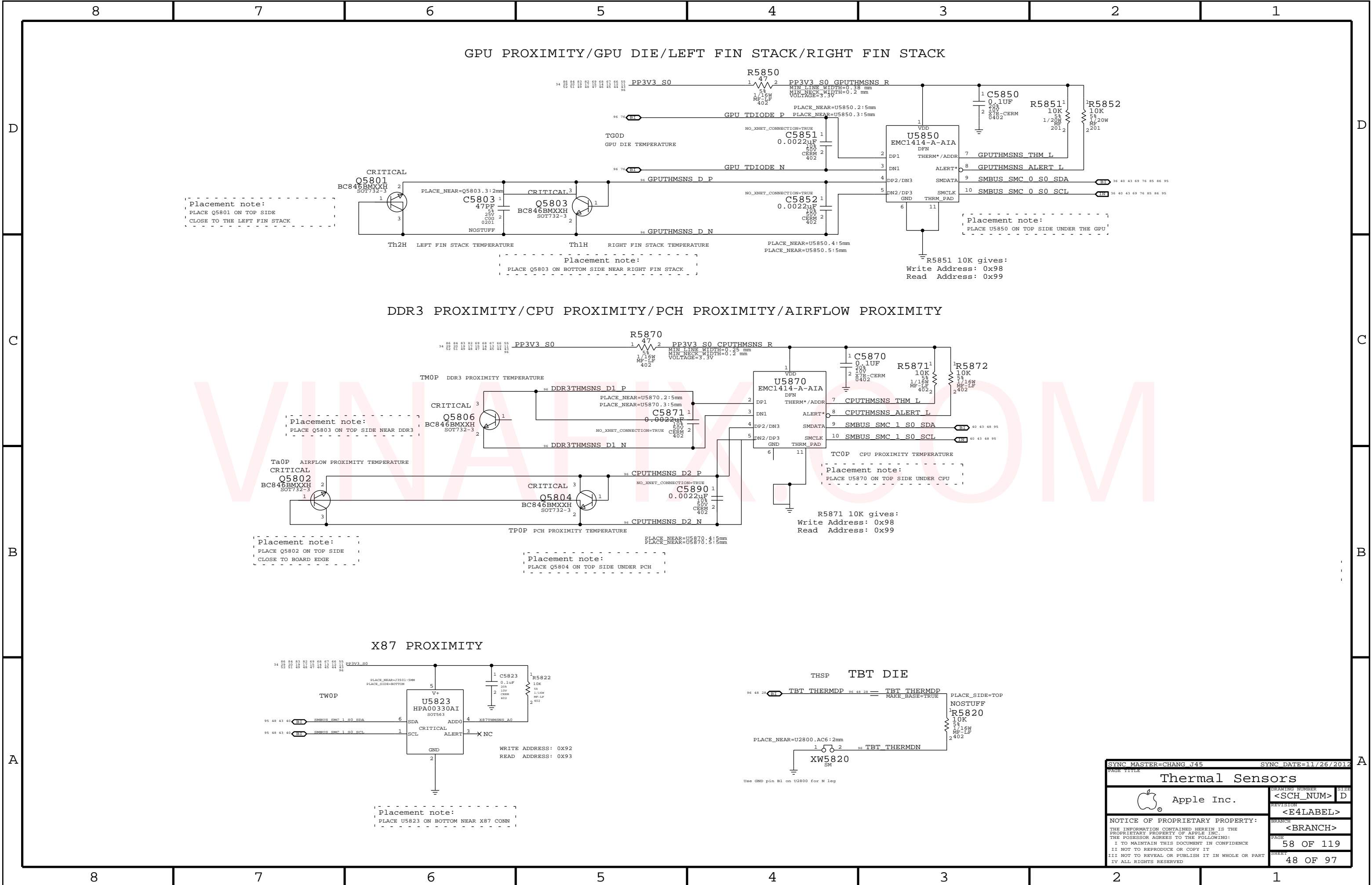



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	5	RES,MTL FILM,100K,5,1/20W,0201,SMD,LF	C5601,C5631,C5600,C5681,C5671		SENSOR_NONPROD:N

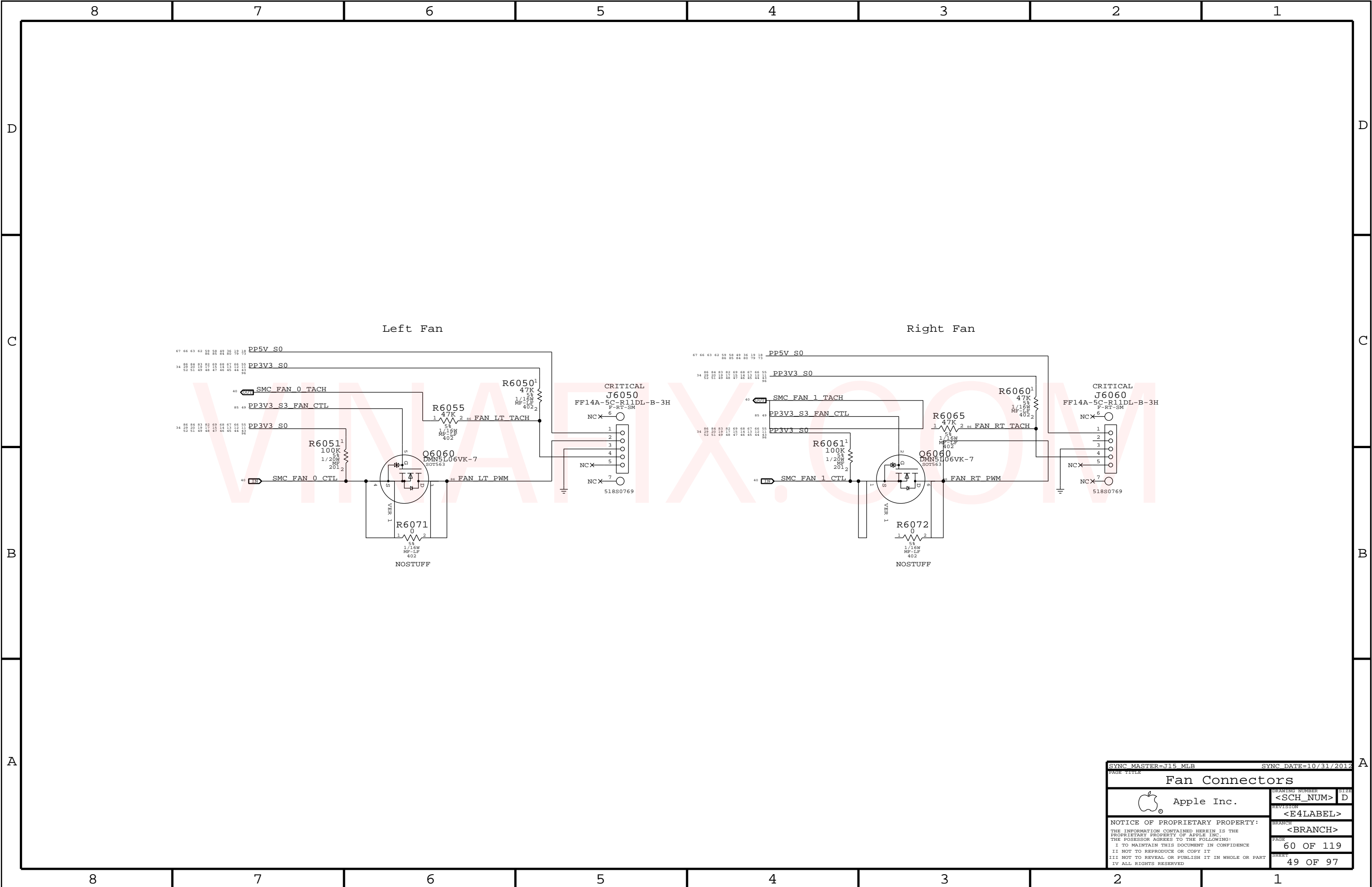


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Debug Sensors	
Apple Inc.	DRAWING NUMBER
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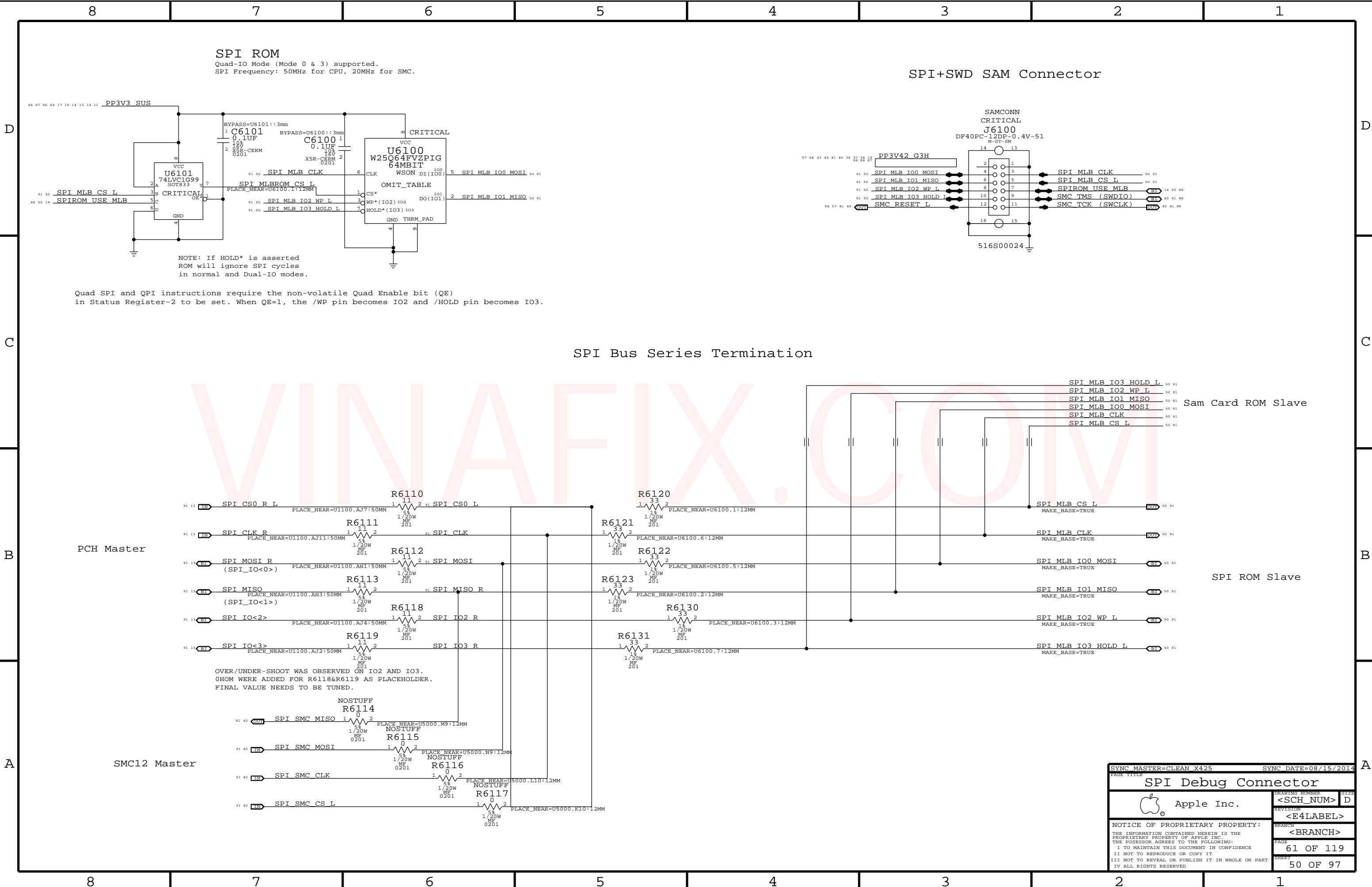




SYNC MASTER=CHANG J45		SYNC DATE=11/26/2012	
PAGE TITLE			
Thermal Sensors			
 Apple Inc.		DRAWING NUMBER	SIZE
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		SHEET	48 OF 97








SPI ROM  
Quad-I/O Mode (Mode 0 & 3) supported.  
SPI Frequency: 50MHz for CPU, 20MHz for SMC.

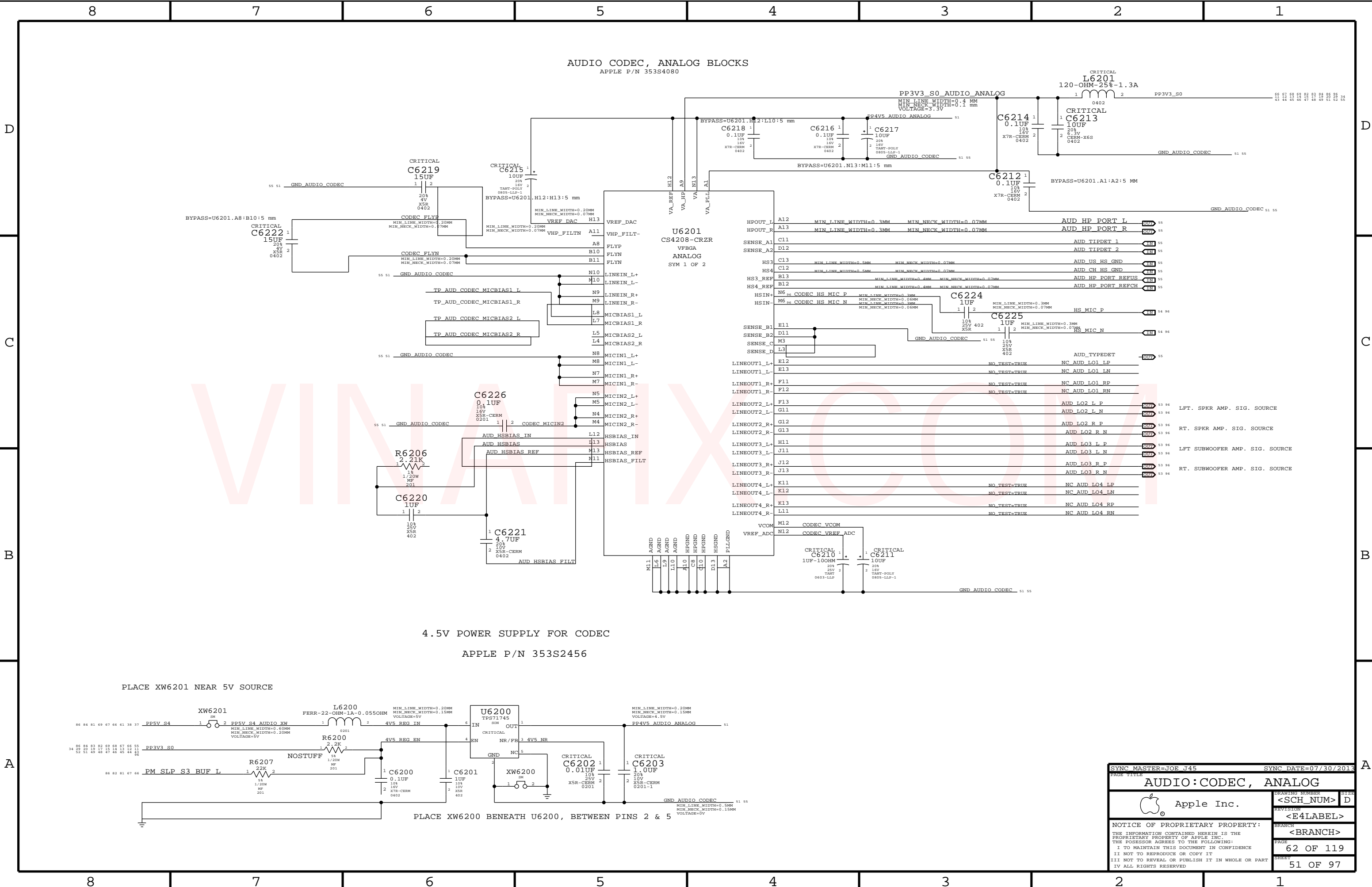
SPI+SWD SAM Connector

SPI Bus Series Termination

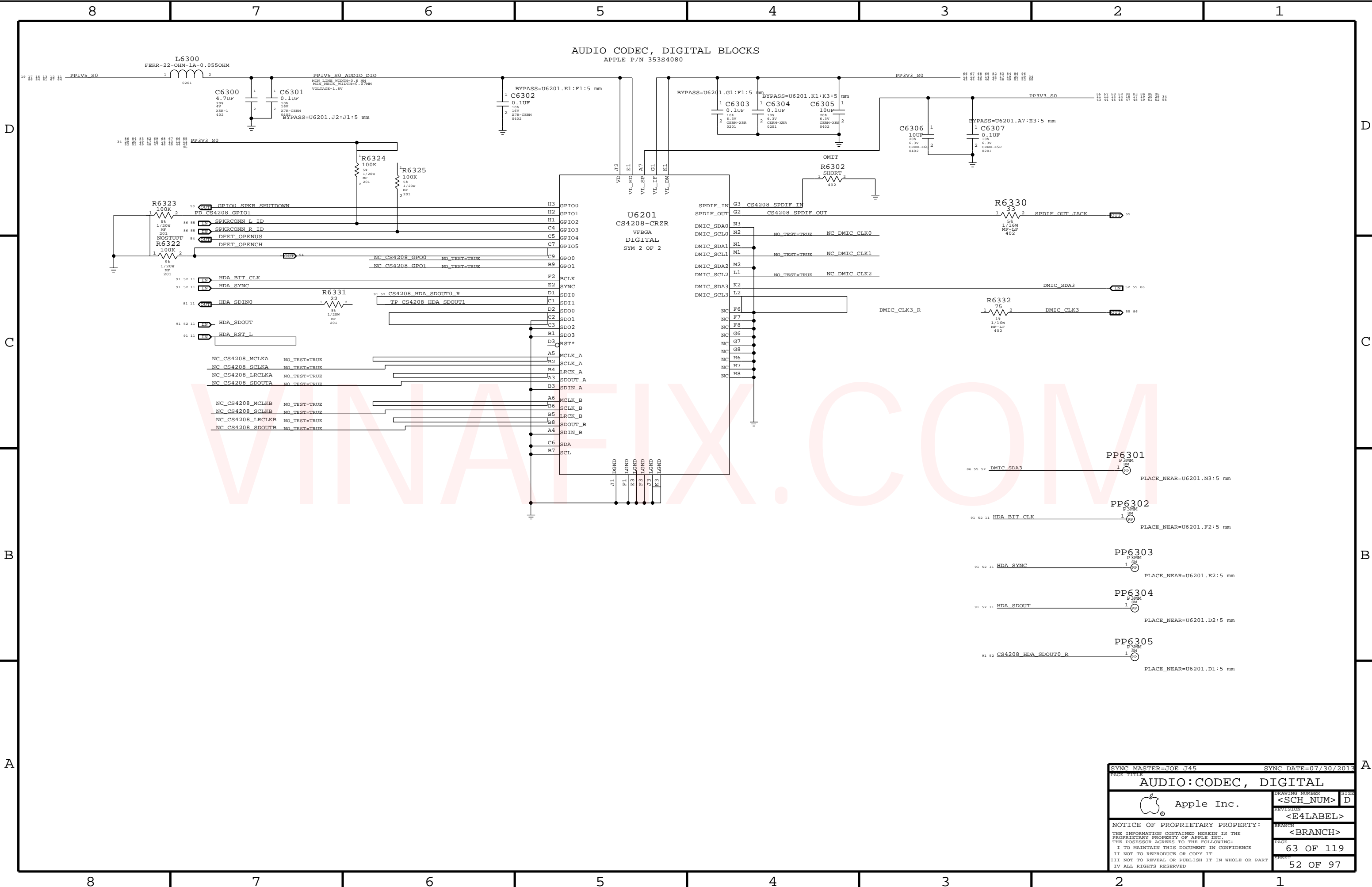
Sam Card ROM Slave

SPI ROM Slave

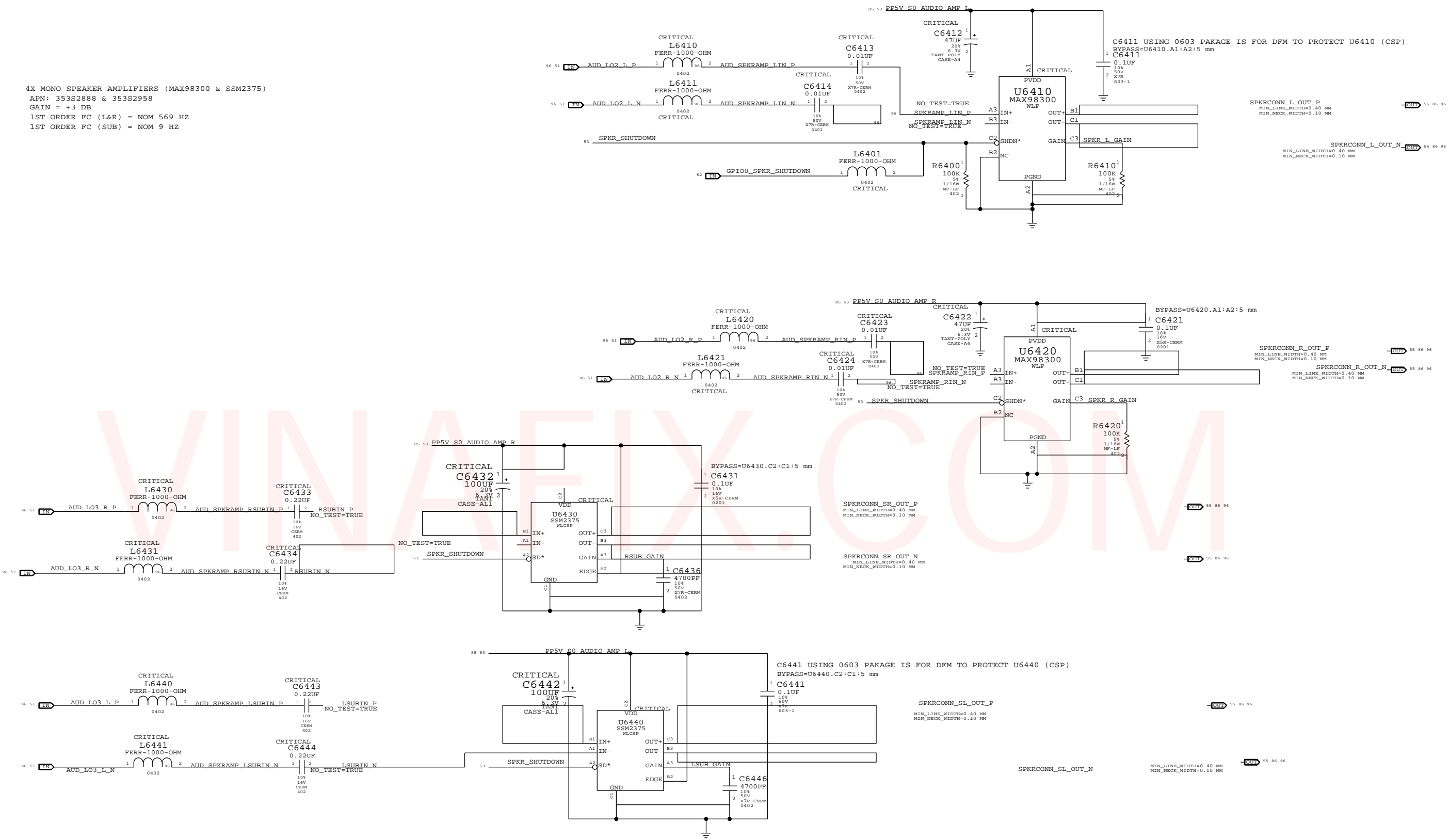
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PAGE TITLE			
SPI Debug Connector			
 Apple Inc.		DRAWING NUMBER	
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SYNC MASTER=JOE J45		SYNC DATE=07/30/2013	
PAGE TITLE		AUDIO:CODEC, ANALOG	
DRAWING NUMBER		SIZE	
<SCH_NUM>		D	
REVISION		BRANCH	
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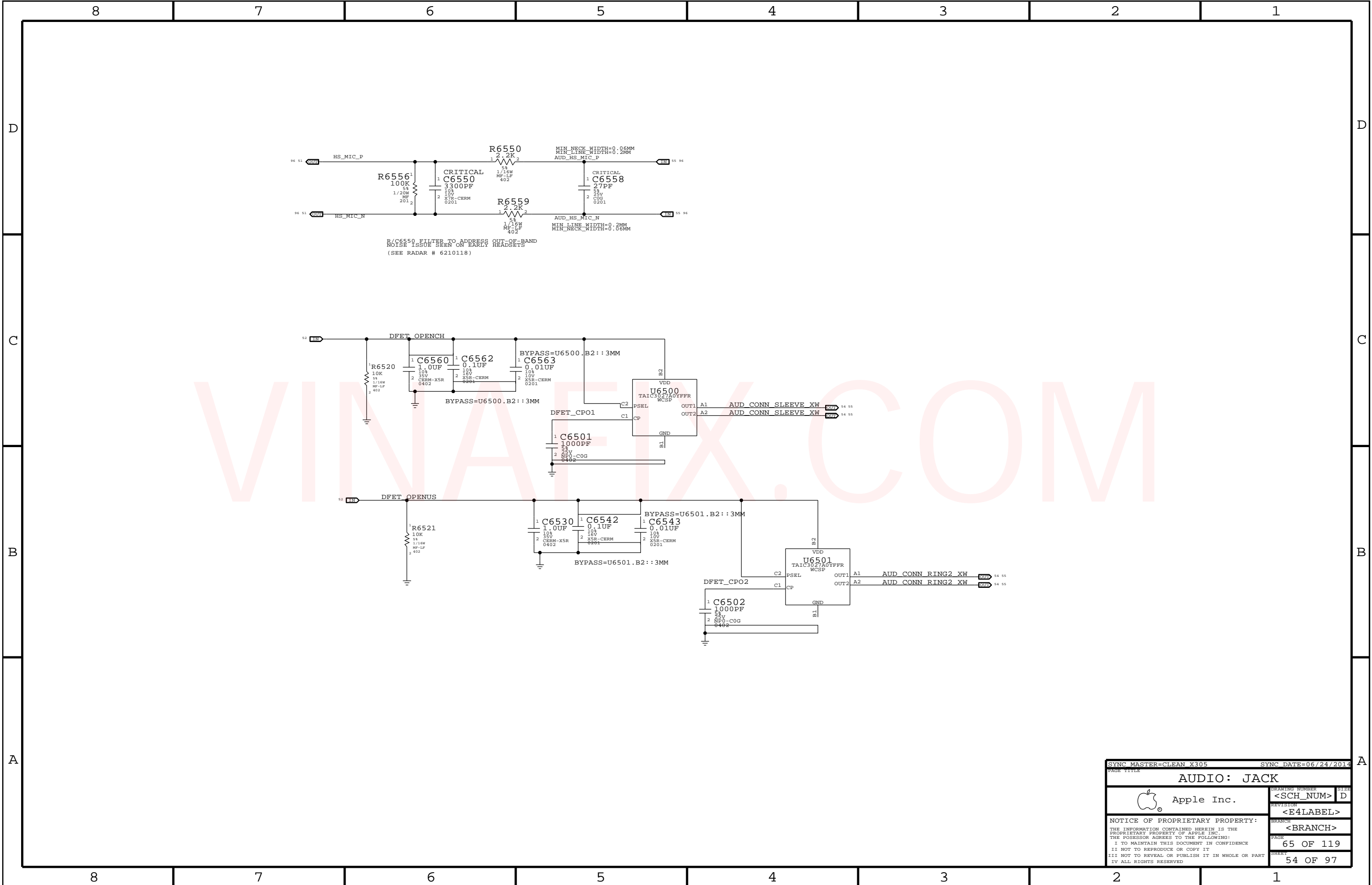


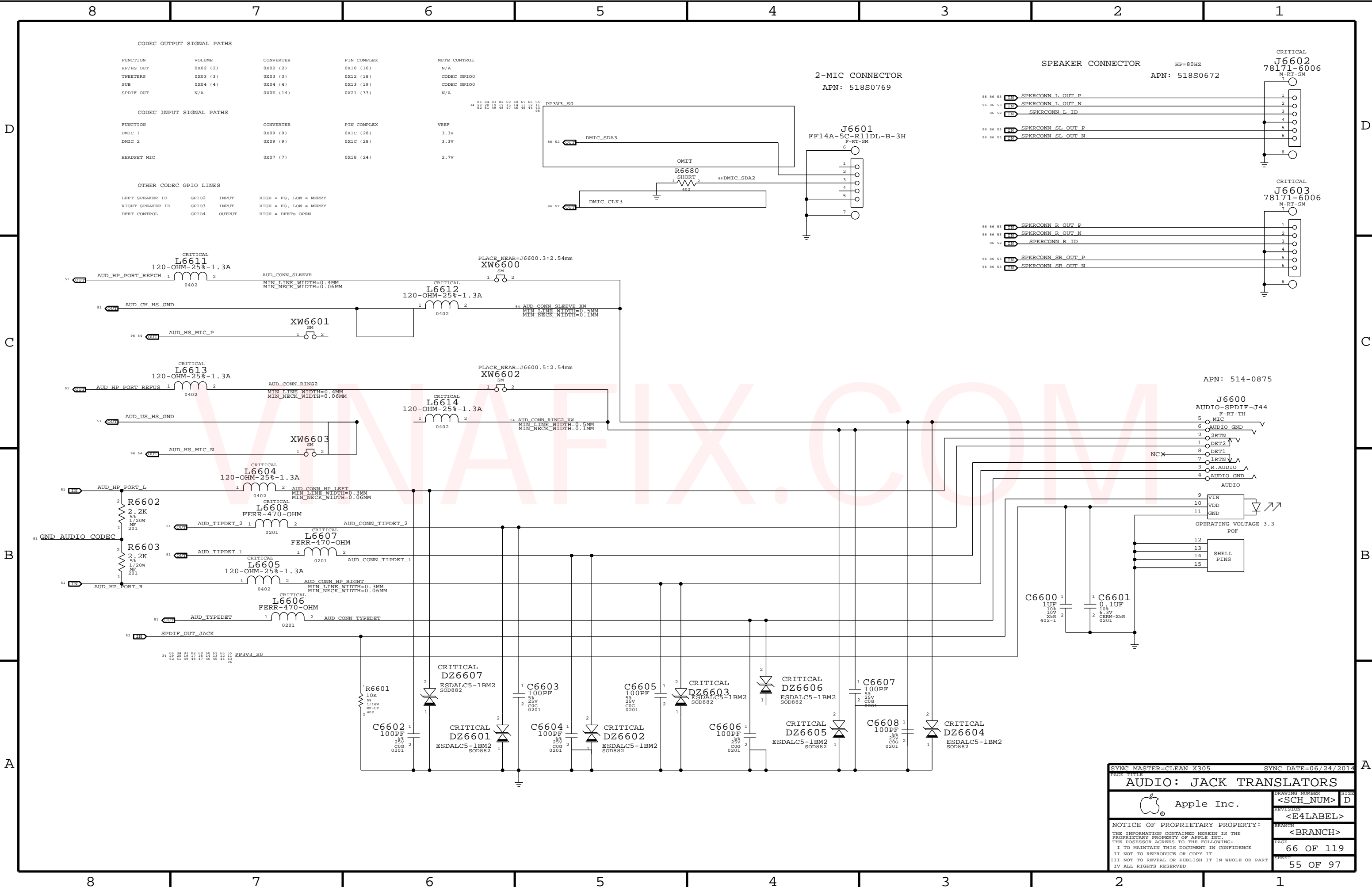
4X MONO SPEAKER AMPLIFIERS (MAX98300 & SSM2375)  
APN: 353S2888 & 353S2958  
GAIN = +3 DB  
1ST ORDER FC (L&R) = NOM 569 HZ  
1ST ORDER FC (SUB) = NOM 9 HZ



SYNC MASTER=JOE J45		SYNC DATE=07/30/2013	
PAGE TITLE			
AUDIO: SPEAKER AMP			
 Apple Inc.		DRAWING NUMBER	SIZE
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		<E4LABEL>	
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		<BRANCH>	
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CODEC OUTPUT SIGNAL PATHS				
FUNCTION	VOLUME	CONVERTER	PIN COMPLEX	MUTE CONTROL
HP/HS OUT	0XD2 (2)	0XD2 (2)	0X10 (16)	N/A
TWEETERS	0XD3 (3)	0XD3 (3)	0X12 (18)	CODEC GPIO0
SUB	0XD4 (4)	0XD4 (4)	0X13 (19)	CODEC GPIO0
SPDIF OUT	N/A	0XD0E (14)	0X21 (33)	N/A

CODEC INPUT SIGNAL PATHS				
FUNCTION	CONVERTER	PIN COMPLEX	VREF	
DMIC 1	0XD09 (9)	0X1C (28)	3.3V	
DMIC 2	0XD09 (9)	0X1C (28)	3.3V	
HEADSET MIC	0XD07 (7)	0X18 (24)	2.7V	

OTHER CODEC GPIO LINES				
LEFT SPEAKER ID	GPIO2	INPUT	HIGH = FG, LOW = MERRY	
RIGHT SPEAKER ID	GPIO3	INPUT	HIGH = FG, LOW = MERRY	
DFET CONTROL	GPIO4	OUTPUT	HIGH = DFETs OPEN	

2-MIC CONNECTOR  
APN: 518S0769

SPEAKER CONNECTOR  
HP=80HZ  
APN: 518S0672

CRITICAL  
J6602  
78171-6006  
M-RT-SM

CRITICAL  
J6603  
78171-6006  
M-RT-SM

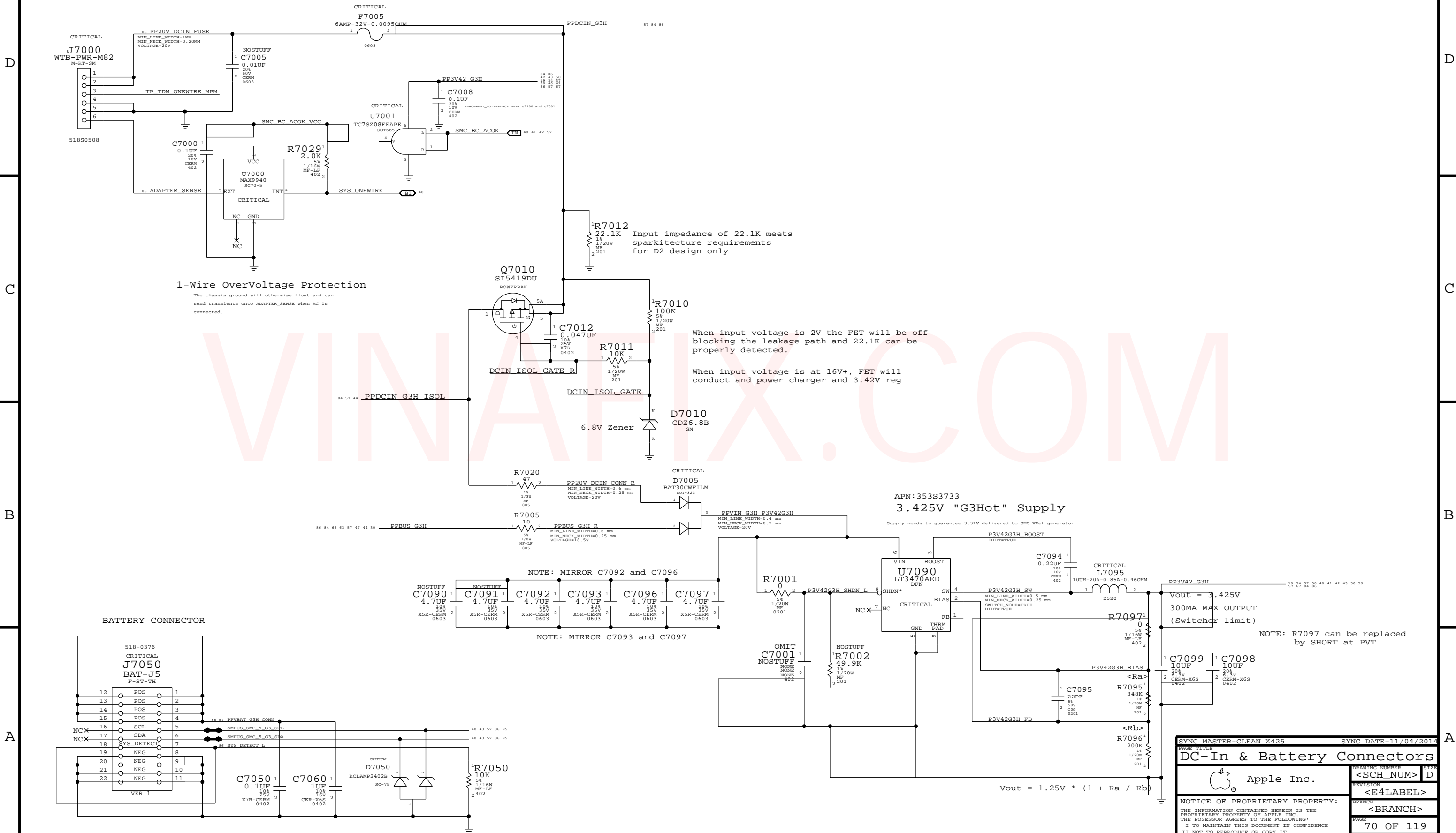
APN: 514-0875

J6600  
AUDIO-SPDIF-J44

PAGE TITLE		SYNC DATE=06/24/2014	
AUDIO: JACK TRANSLATORS			
Apple Inc.		DRAWING NUMBER	SIZE
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		PAGE	66 OF 119
		SHEET	55 OF 97

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MagSafe DC Power Jack



1-Wire OverVoltage Protection

The chassis ground will otherwise float and can send transients onto ADAPTER\_SENSE when AC is connected.

Input impedance of 22.1K meets sparkiterture requirements for D2 design only

When input voltage is 2V the FET will be off blocking the leakage path and 22.1K can be properly detected.

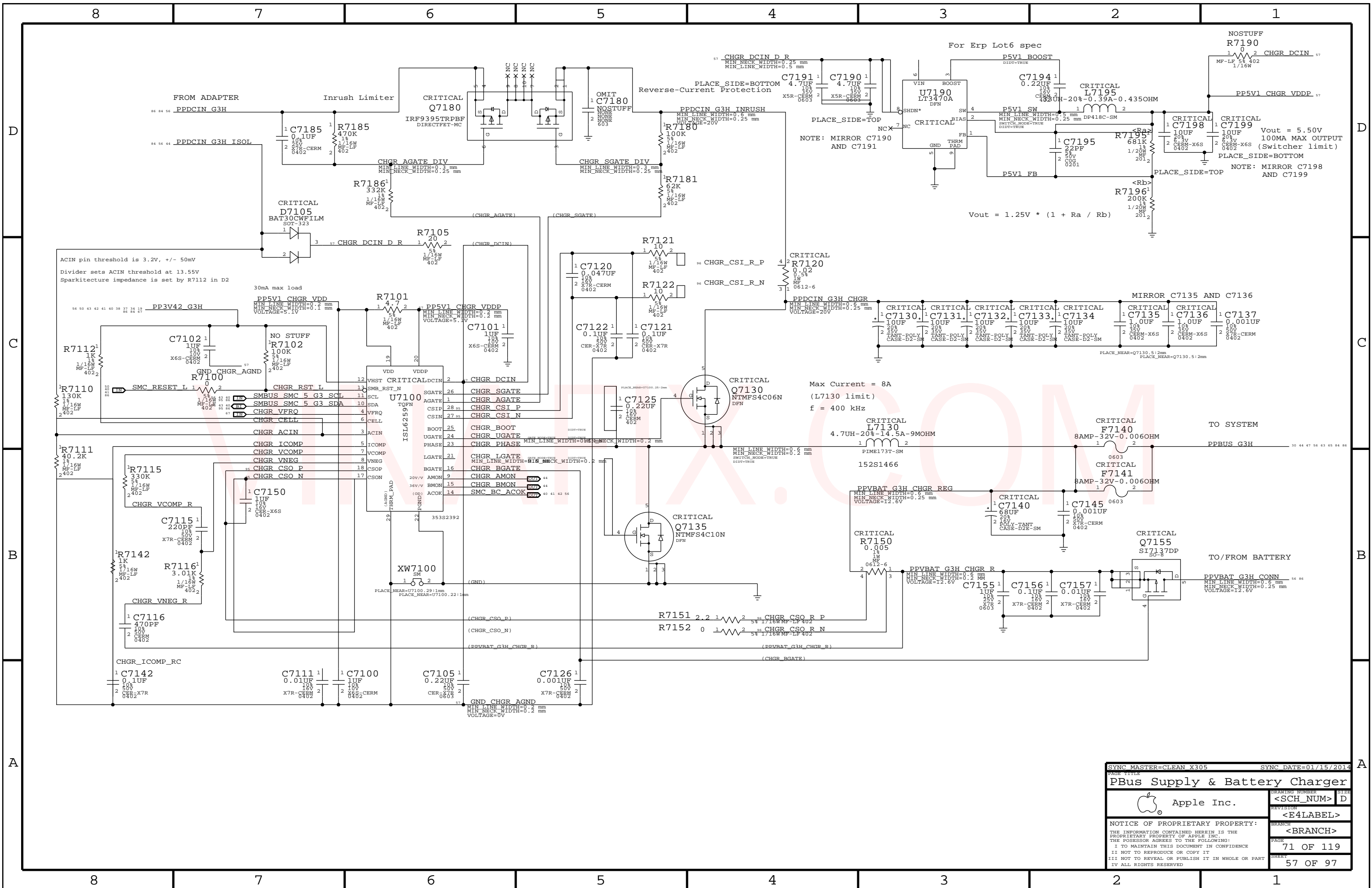
When input voltage is at 16V+, FET will conduct and power charger and 3.42V reg


3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC Vref generator

NOTE: R7097 can be replaced by SHORT at PVT

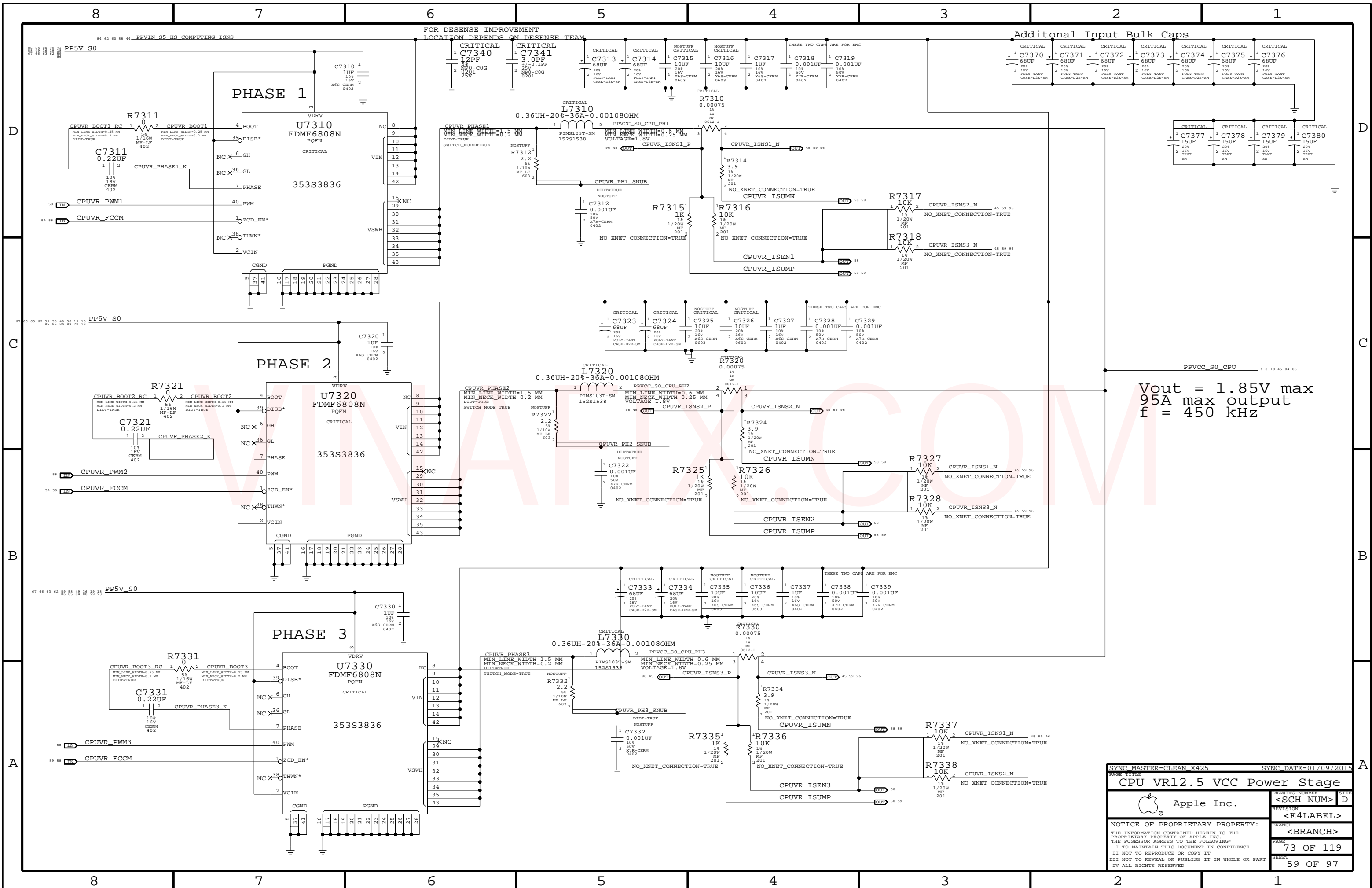
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PAGE TITLE		DC-In & Battery Connectors	
Apple Inc.		DRAWING NUMBER	SIZE
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		REVISION	
		<E4LABEL>	
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SYNC MASTER=CLEAN X305		SYNC DATE=01/15/2014	
PAGE TITLE			
PBus Supply & Battery Charger			
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	REVISION		
	<E4LABEL>		
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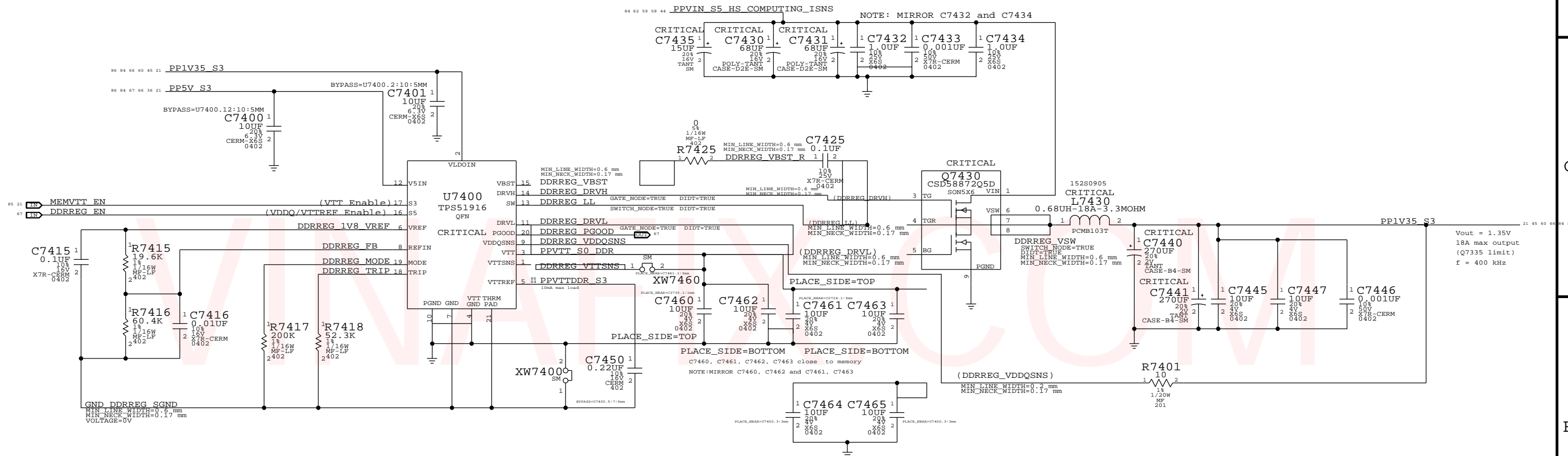





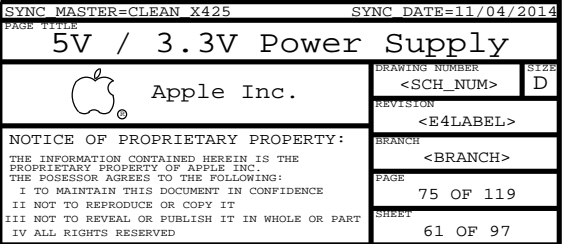


SYNC MASTER=CLEAN X425		SYNC DATE=01/09/2015	
PAGE TITLE			
CPU VR12.5 VCC Power Stage			
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Apple Inc.		<SCH_NUM>	D
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DDR3L (1V35 S3) REGULATOR

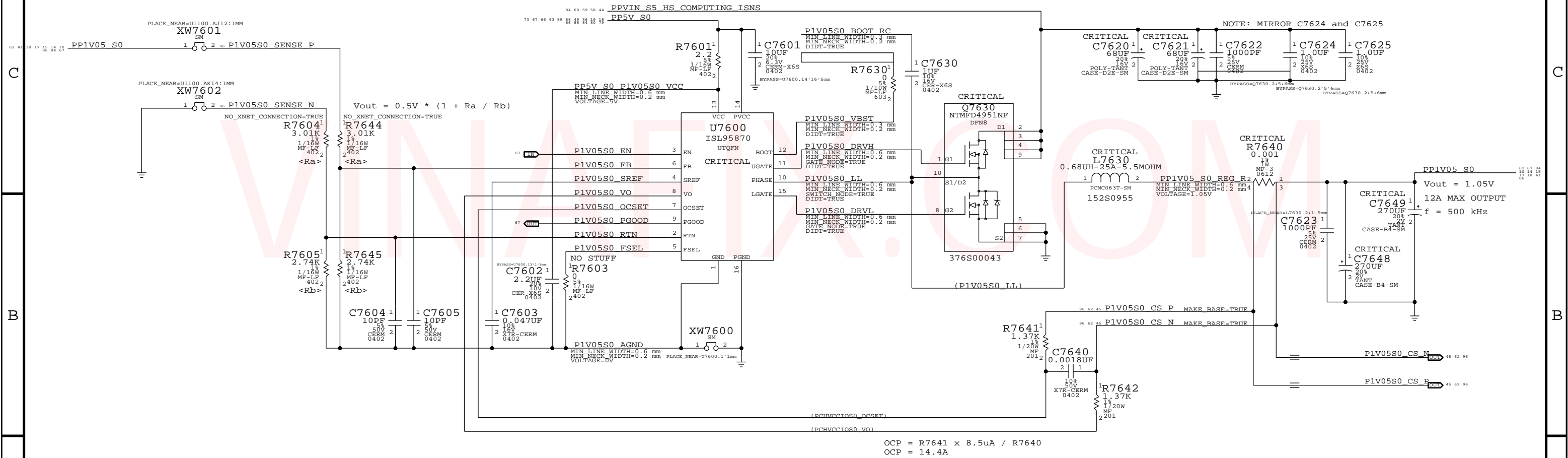


SYNC MASTER=CLEAN X305		SYNC DATE=01/15/2014	
PAGE TITLE			
1.35V DDR3L SUPPLY			
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	REVISION		
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	PAGE		<BRANCH>
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SHEET		60 OF 97	






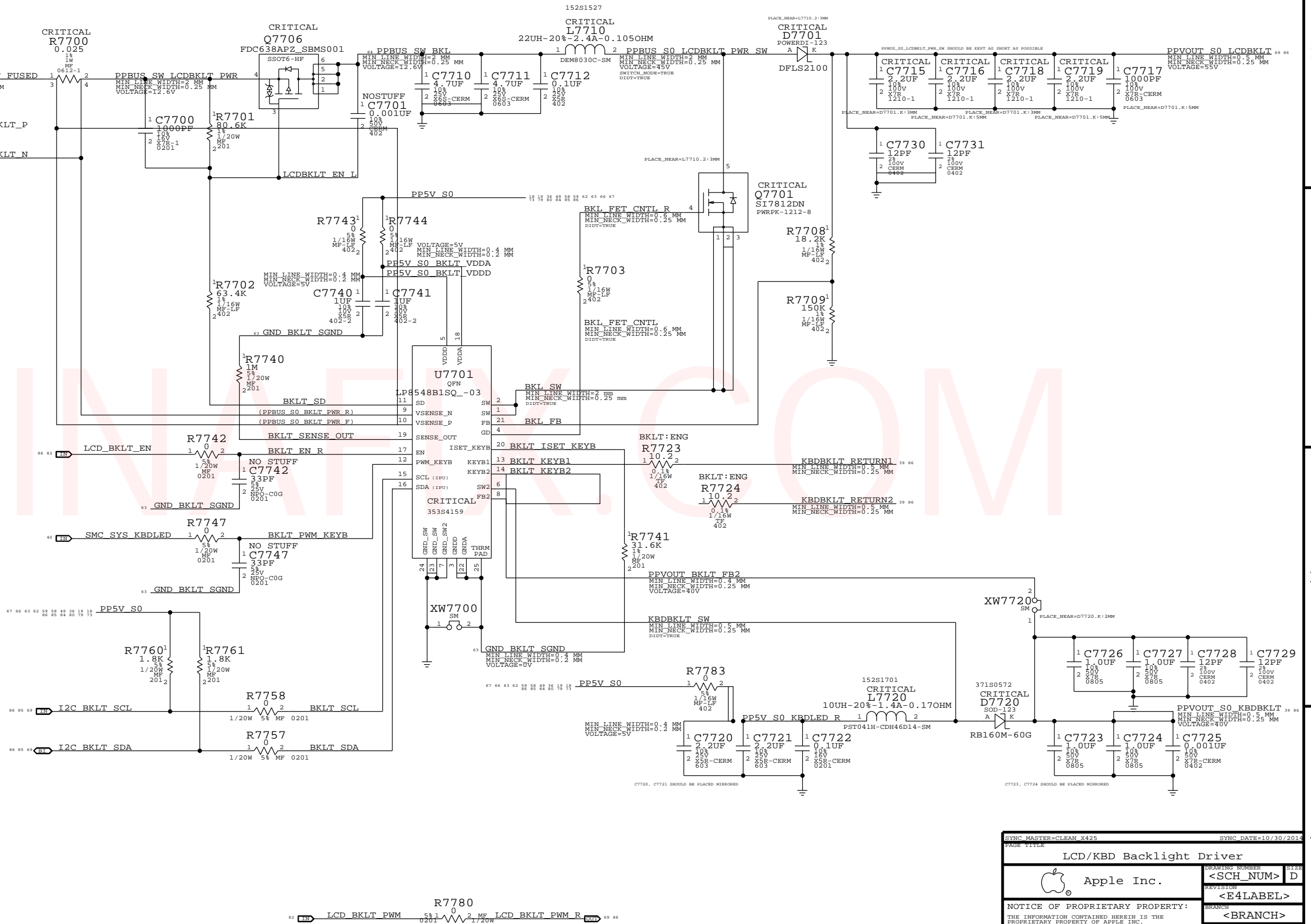
1V05 S0 REGULATOR




OCF = R7641 x 8.5uA / R7640  
OCF = 14.4A

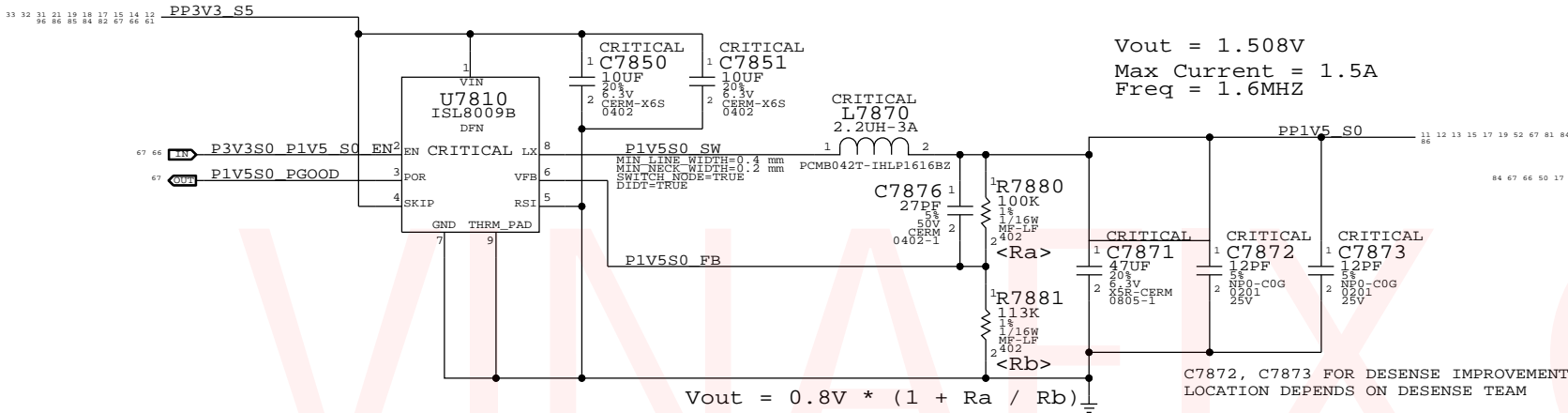
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1V05V POWER SUPPLY				
	DRAWING NUMBER		SIZE	
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	REVISION		<E4LABEL>	
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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	2	RES,MTL FILM, 0 OHM,1A MAX,0402,SMD	R7723,R7724		BKLT:PROD



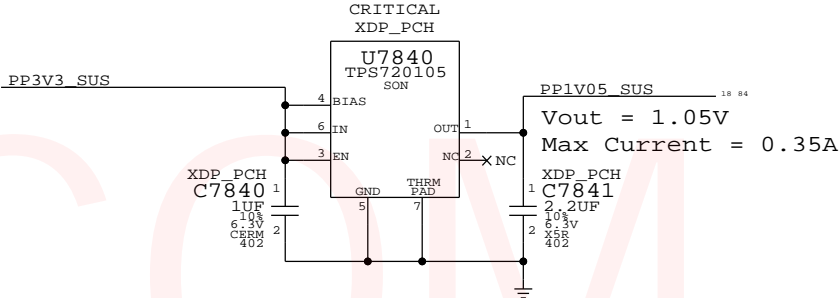
SYNC MASTER=CLEAN X425		SYNC DATE=19/30/2014	
PAGE TITLE			
LCD/KBD Backlight Driver			
 Apple Inc.		DRAWING NUMBER <b>&lt;SCH_NUM&gt; D</b>	
		REVISION <b>&lt;E4LABEL&gt;</b>	
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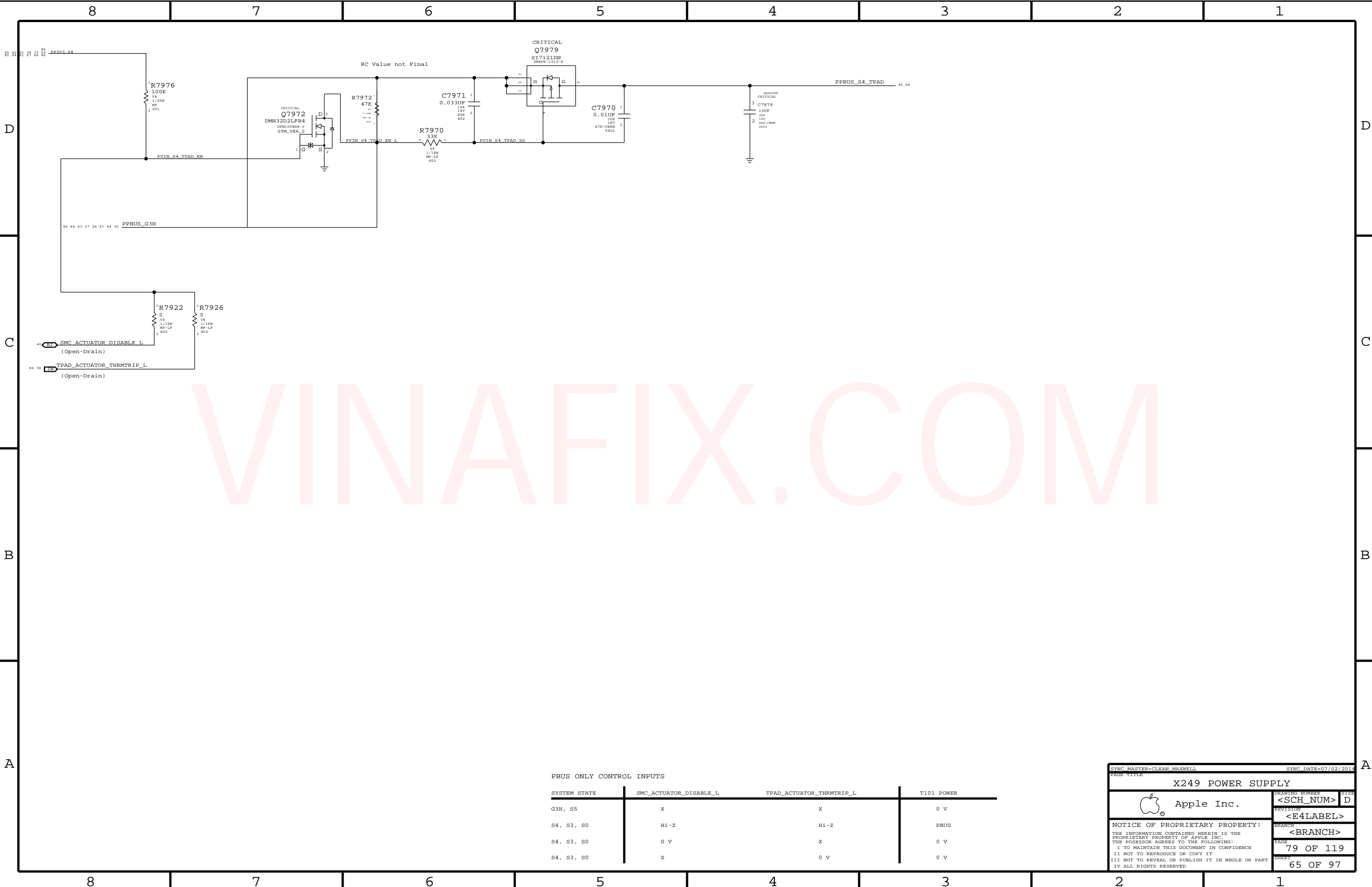
1.5V S0 Regulator



1.05V SUS LDO

Lynx Point-H requires JTAG pull-ups to be powered at 1.05V in SUS.  
Pull-ups (3) must be 51 ohms to support XDP (not required in production).  
70mA is required to support pull-ups. Alternative is strong voltage  
dividers (200/100) to 3.3V SUS, which burns 100mW in all S-states.






PBUS ONLY CONTROL INPUTS

SYSTEM STATE	SMC_ACTUATOR_DISABLE_L	TPAD_ACTUATOR_THRMTRIP_L	T101 POWER
G3H, S5	X	X	0 V
S4, S3, S0	Hi-Z	Hi-Z	PBUS
S4, S3, S0	0 V	X	0 V
S4, S3, S0	X	0 V	0 V

SYNC MASTER=CLEAN MAXWELL

SYNC DATE=07/02/2014

X249 POWER SUPPLY

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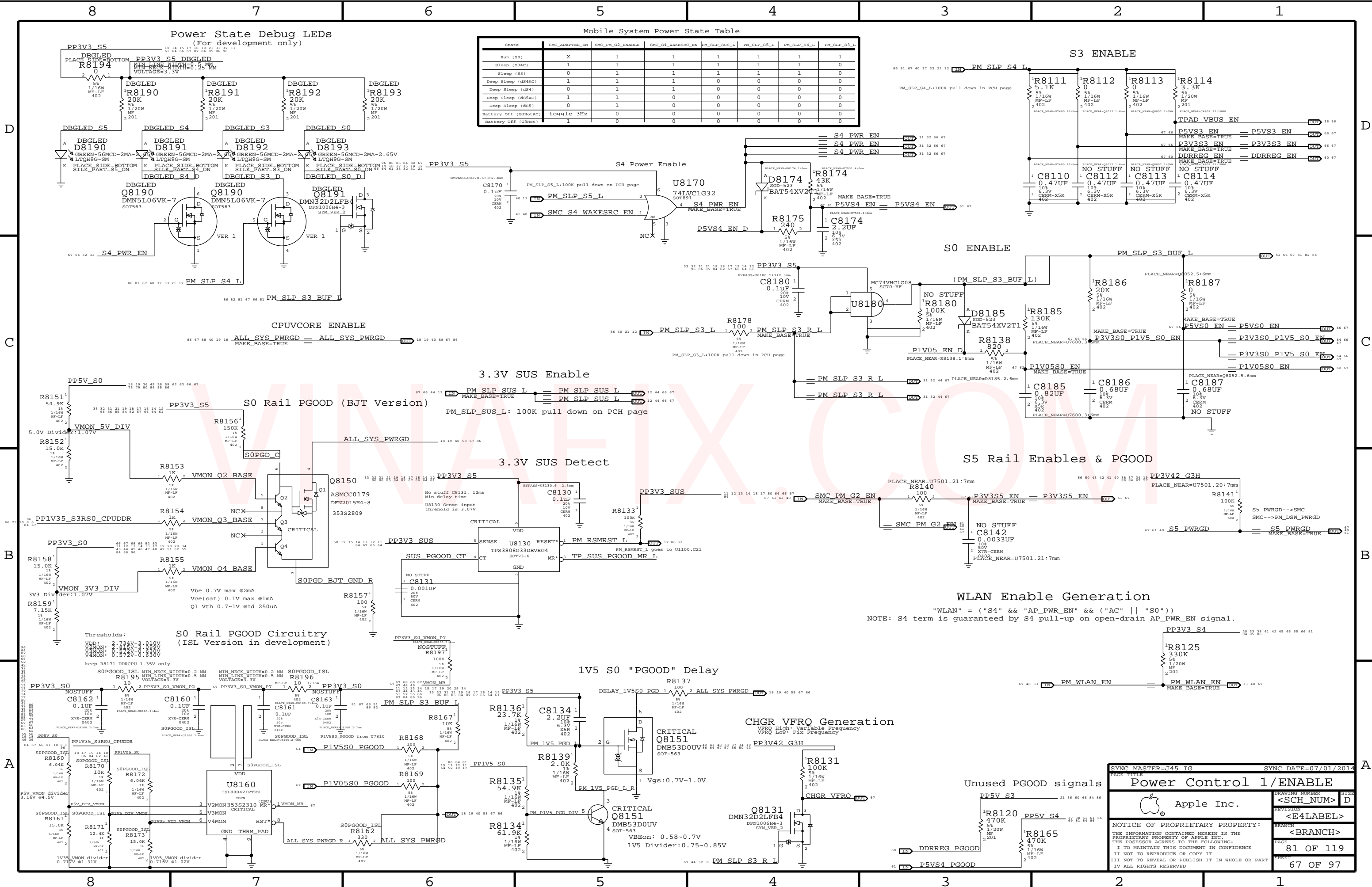
PAGE  
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SHEET  
65 OF 97

SIZE  
D







Mobile System Power State Table						
State	SMC_ADAPTER_EN	SMC_PM_G2_ENABLE	SMC_S4_WAKESRC_EN	PM_SLP_S5_L	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	X	1	1	1	1	1
Sleep (S3AC)	1	1	1	1	1	0
Sleep (S3)	0	1	1	1	1	0
Deep Sleep (dS4C)	1	1	1	0	0	0
Deep Sleep (dS4)	0	1	1	0	0	0
Deep Sleep (dS4C)	1	1	0	0	0	0
Deep Sleep (dS5)	1	1	0	0	0	0
Battery Off (G3HotAC)	toggle 3Hz	0	0	0	0	0
Battery Off (G3Hot)	1	0	0	0	0	0

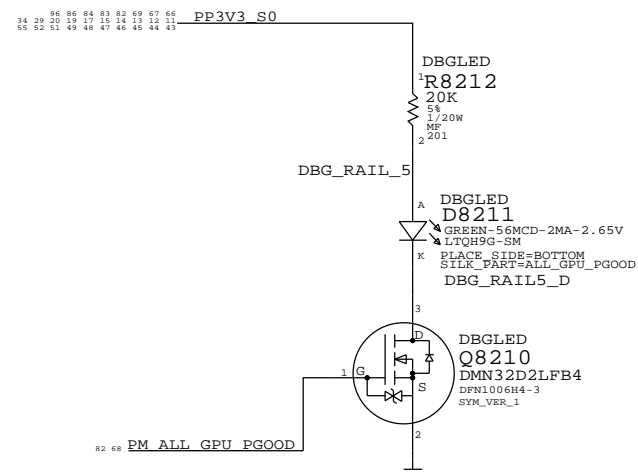
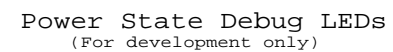
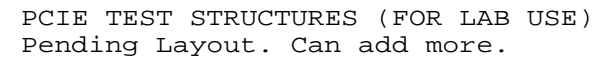
SYNC MASTER=J45\_IG


SYNC DATE=07/01/2014

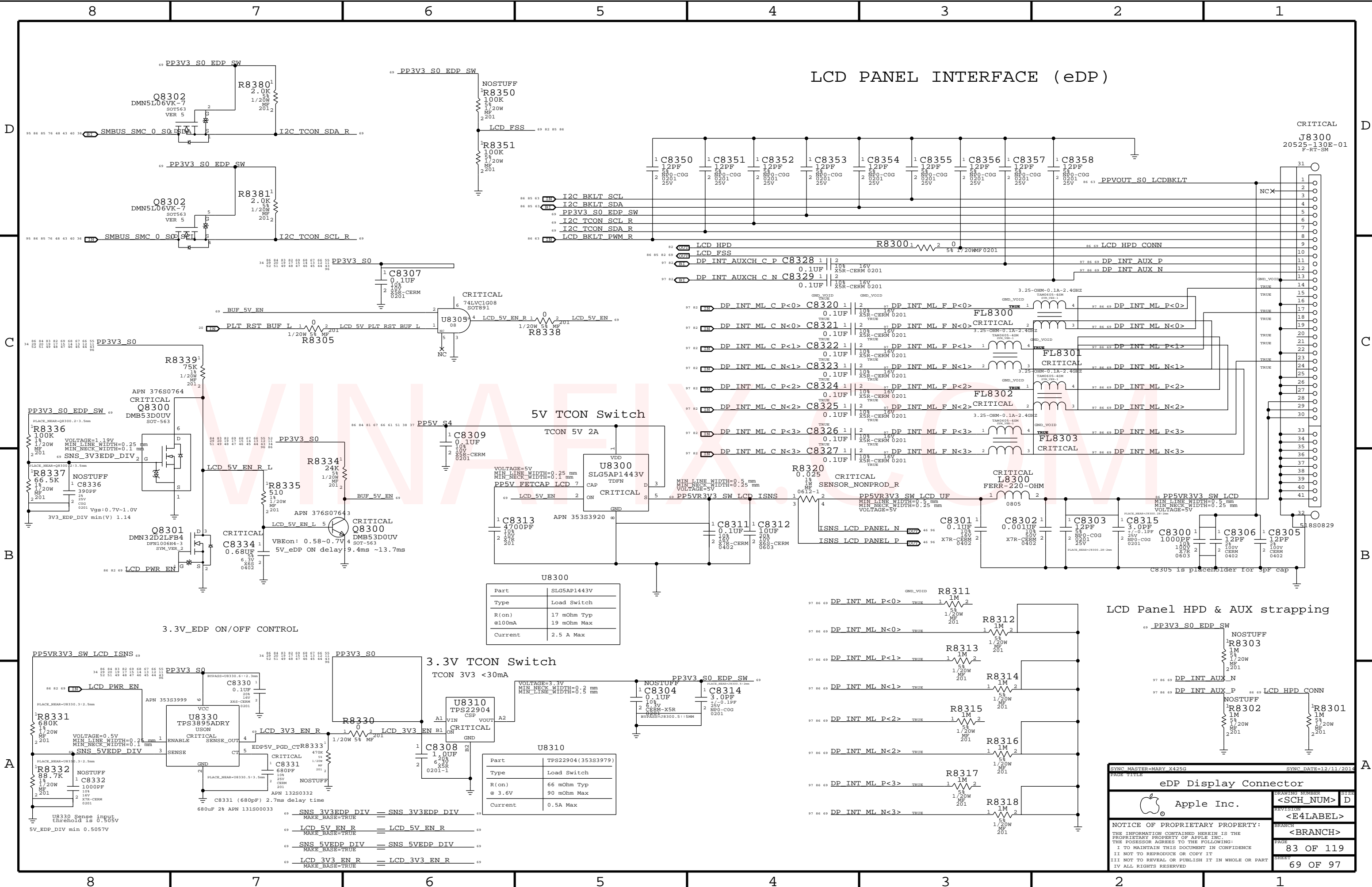
Power Control 1/ENABLE	
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Venus GPU requires rails to come up in the following order:

- 1) GPU\_3.3V
- 2) GPU\_0V95 (BIF\_VDDC) & GPU\_1V8 (VDD\_CT)
- 3) GPUVCORE
- 4) VDDCI
- 5) FB VRAM MVDD



SYNC MASTER=MARY X425G		SYNC DATE=09/11/2014	
PAGE TITLE			
Power Sequencing EG/PGOOD			
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LCD PANEL INTERFACE (eDP)

CRITICAL  
J8300  
20525-130E-01  
F-RT-SM

5V TCON Switch

Part	SLG5AP1443V
Type	Load Switch
R(on)	17 mOhm Typ 19 mOhm Max
Current	2.5 A Max

3.3V TCON Switch

Part	TPS22904(353S3979)
Type	Load Switch
R(on)	66 mOhm Typ 90 mOhm Max
Current	0.5A Max

3.3V\_EDP ON/OFF CONTROL

LCD Panel HPD & AUX strapping

SYNC MASTER=MARY X425G

SYNC DATE=12/11/2014

Apple Inc.

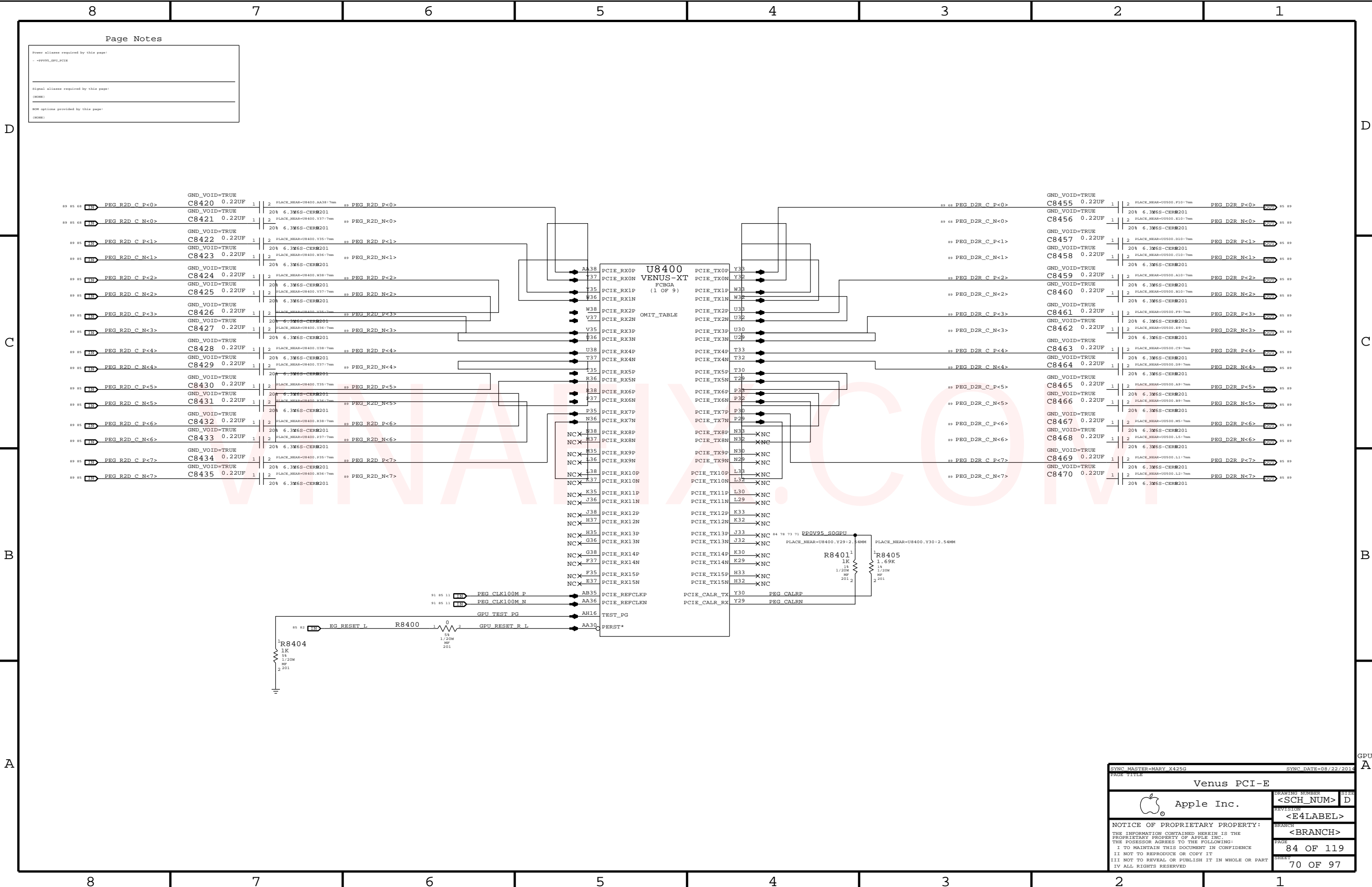
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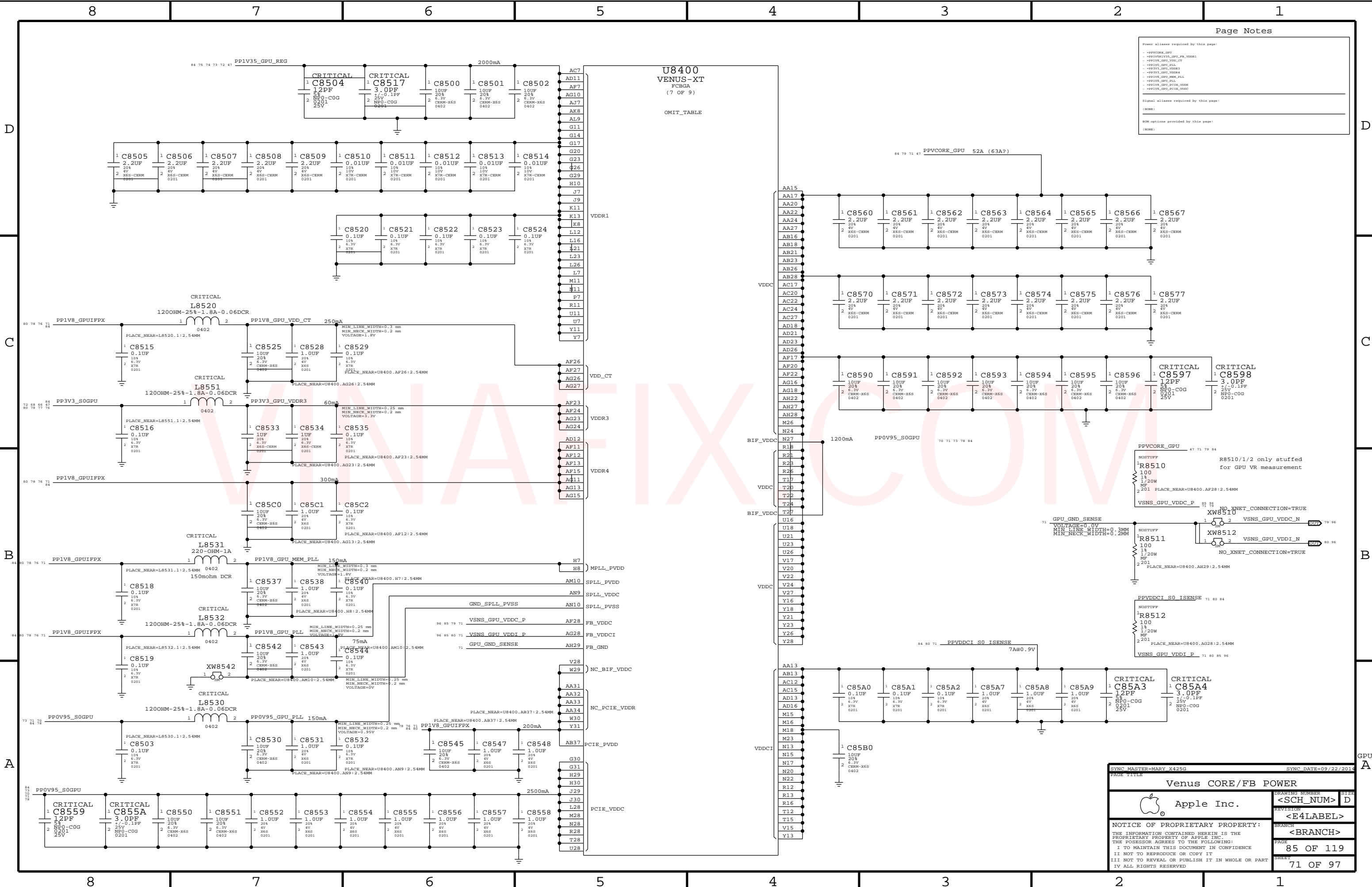
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Signal aliases required by this page:  
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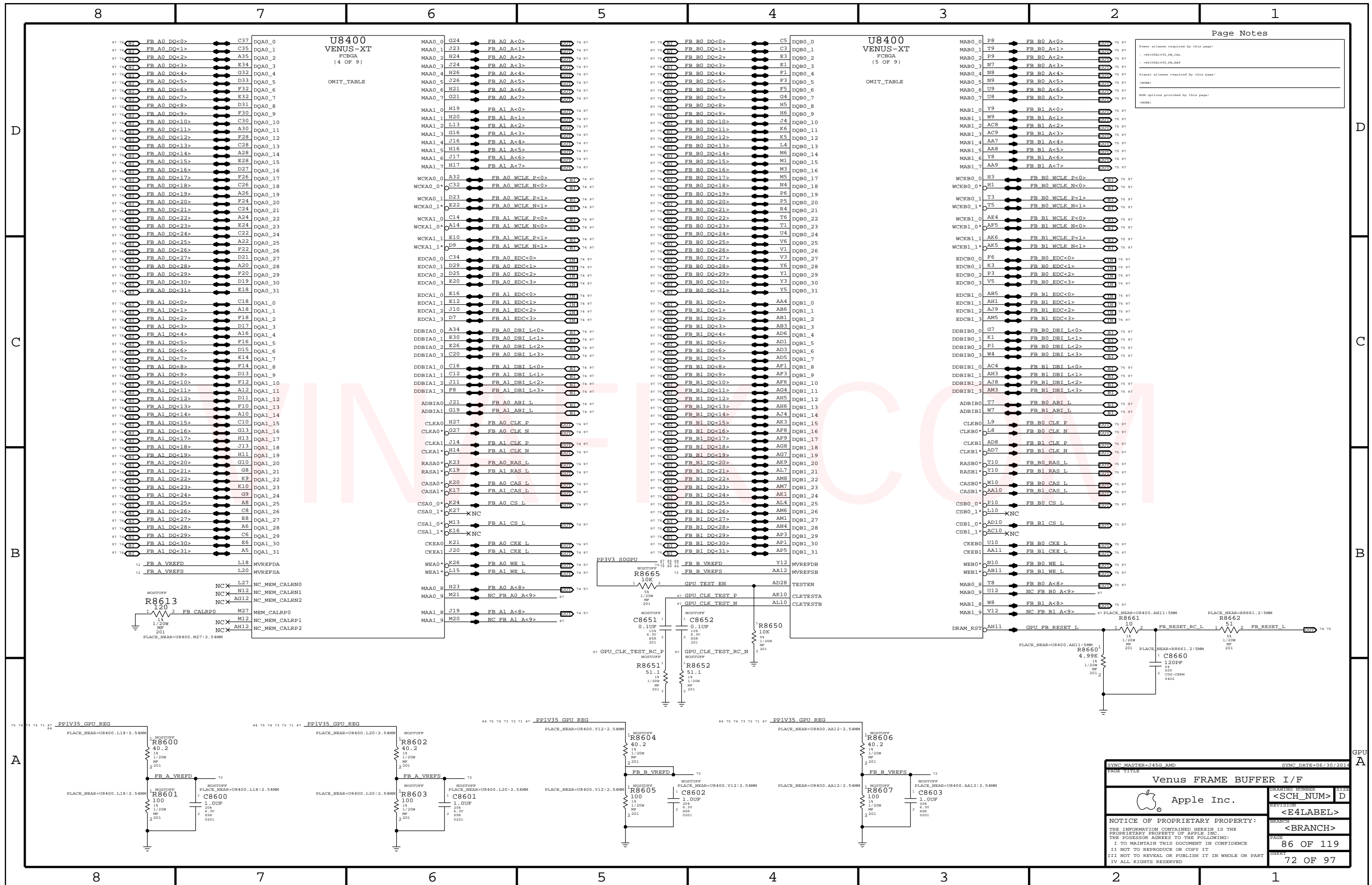
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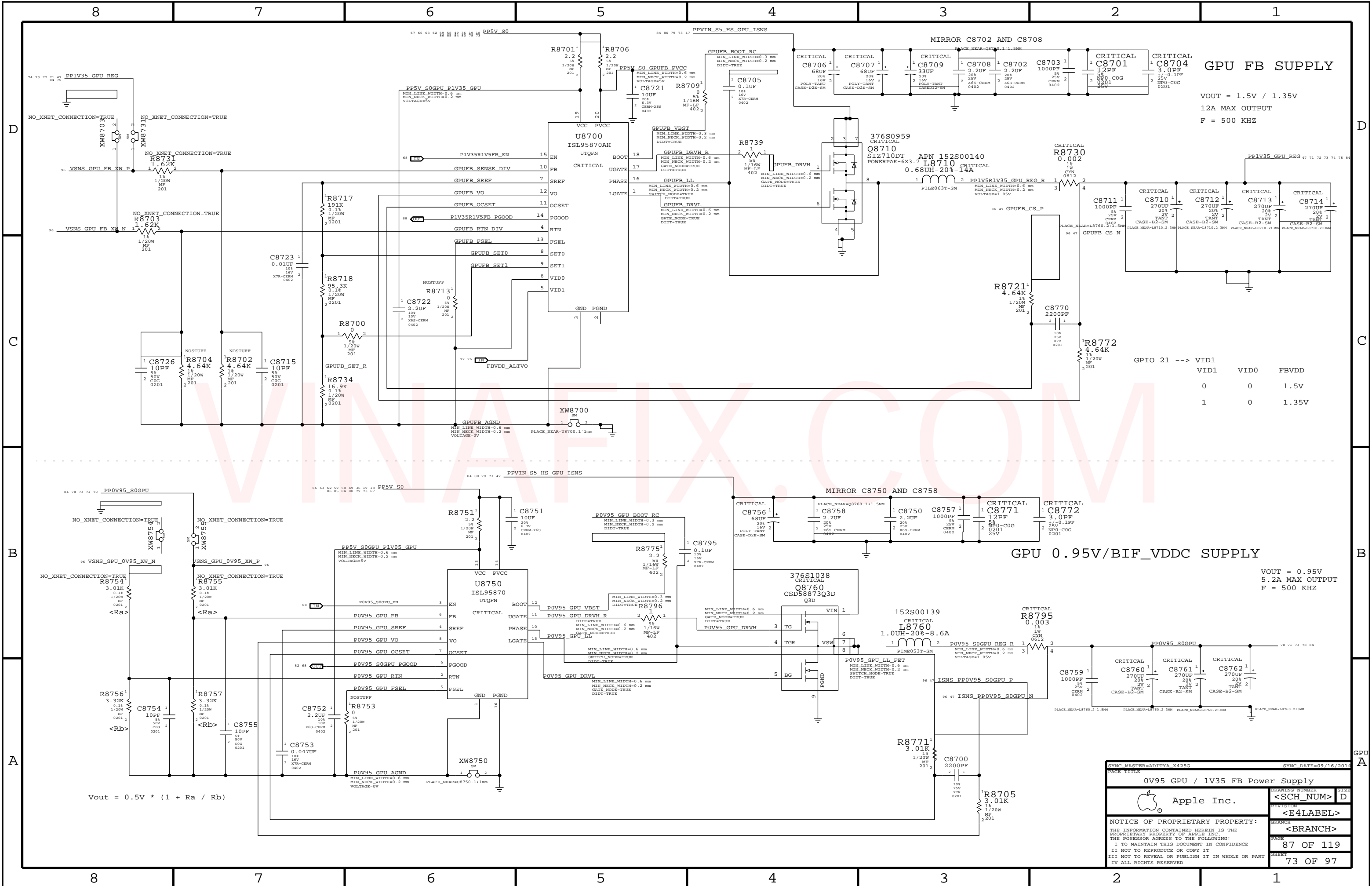




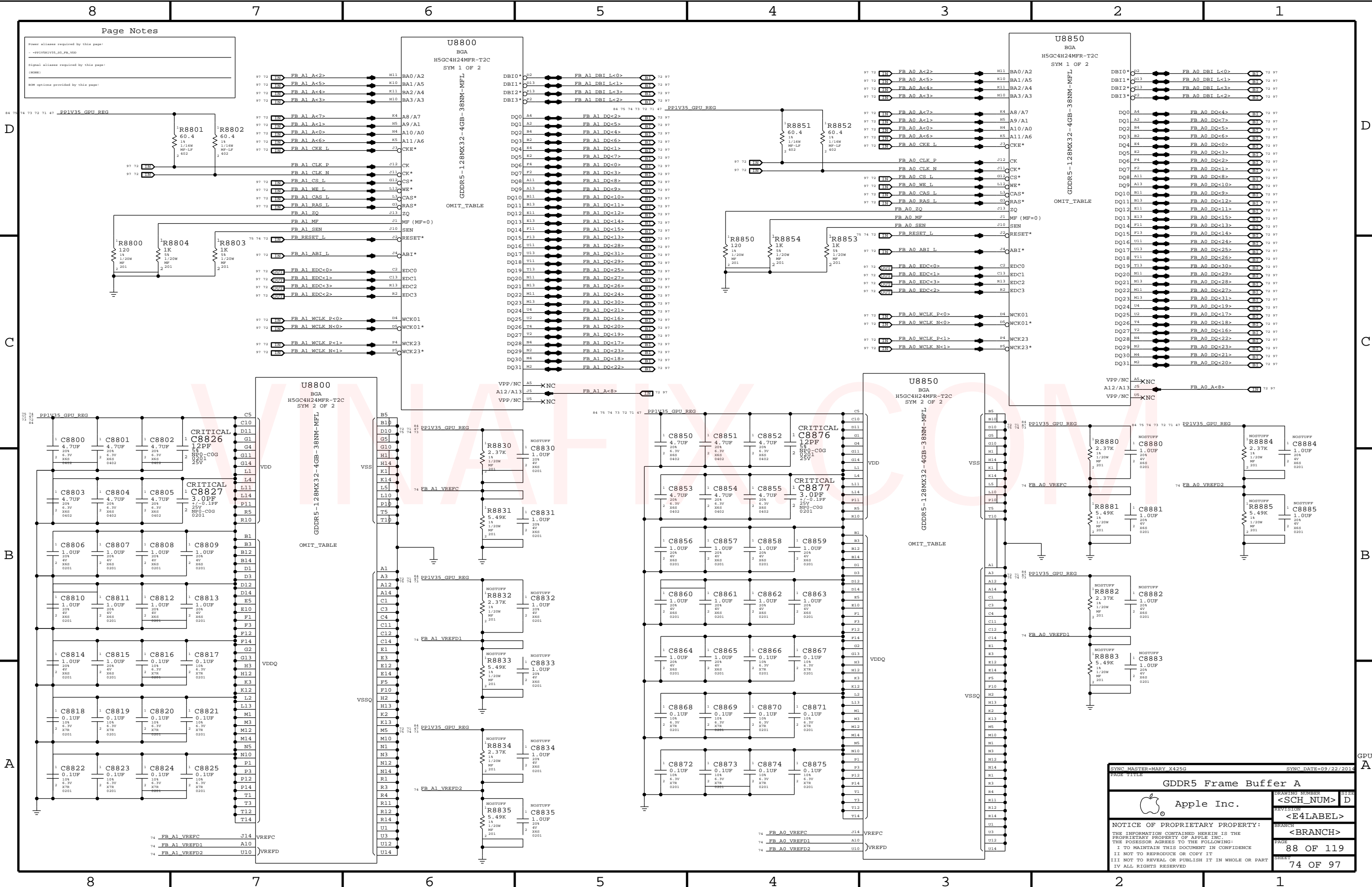
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- PP1V35_GPU_VDD5	
- PP1V35_GPU_VDD6	
- PP1V35_GPU_VDD7	
- PP1V35_GPU_VDD8	
- PP1V35_GPU_VDD9	
- PP1V35_GPU_VDD10	
- PP1V35_GPU_VDD11	
- PP1V35_GPU_VDD12	
- PP1V35_GPU_VDD13	
- PP1V35_GPU_VDD14	
- PP1V35_GPU_VDD15	
- PP1V35_GPU_VDD16	
- PP1V35_GPU_VDD17	
- PP1V35_GPU_VDD18	
- PP1V35_GPU_VDD19	
- PP1V35_GPU_VDD20	
- PP1V35_GPU_VDD21	
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- PP1V35_GPU_VDD98	
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- PP1V35_GPU_VDD100	
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Page Notes

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- ~PPIV35\_GPU\_REG

Signal aliases required by this page:  
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SNM options provided by this page:

U8800  
BGA  
H5GC4H24MFR-T2C  
SYM 1 OF 2

U8850  
BGA  
H5GC4H24MFR-T2C  
SYM 1 OF 2

OMIT\_TABLE

OMIT\_TABLE

U8800  
BGA  
H5GC4H24MFR-T2C  
SYM 2 OF 2

U8850  
BGA  
H5GC4H24MFR-T2C  
SYM 2 OF 2

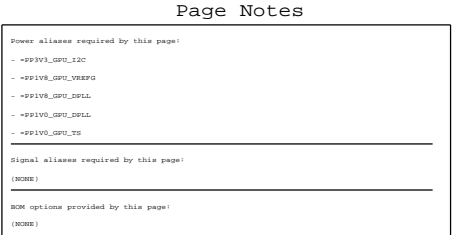
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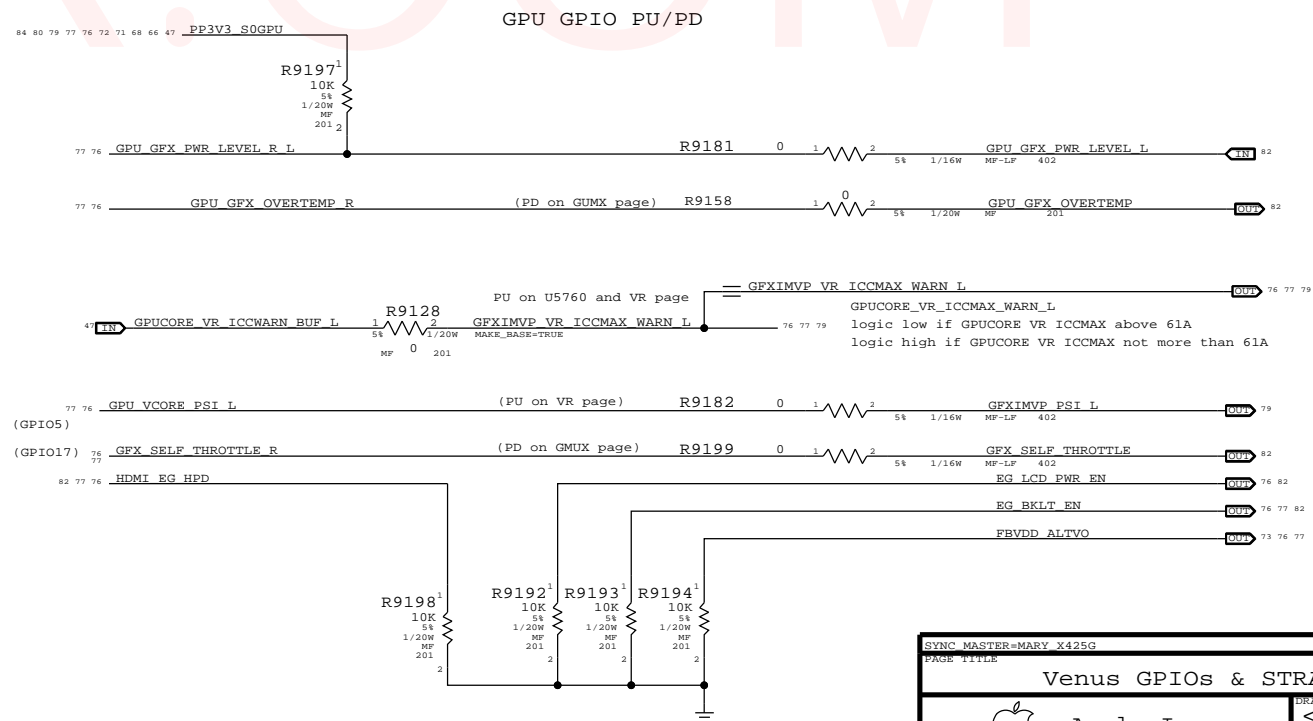
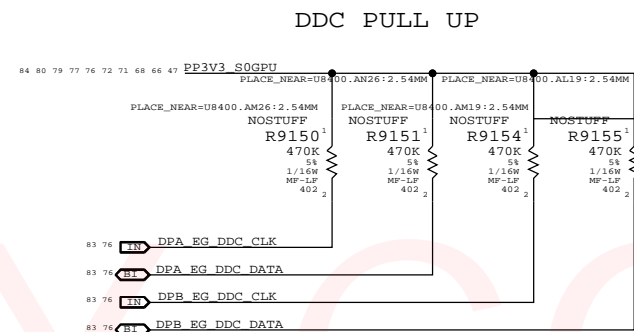
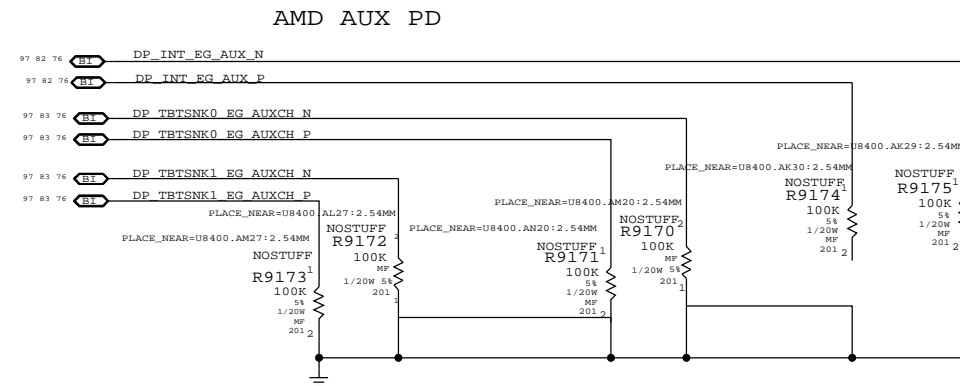
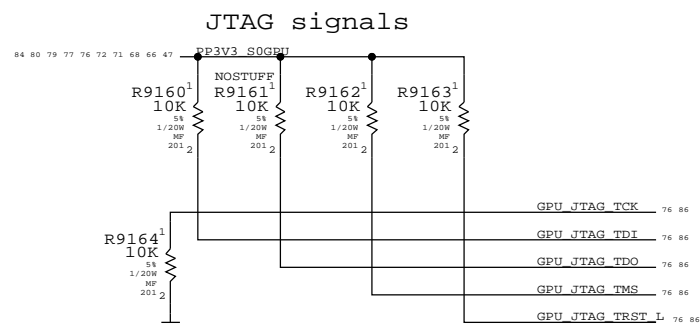
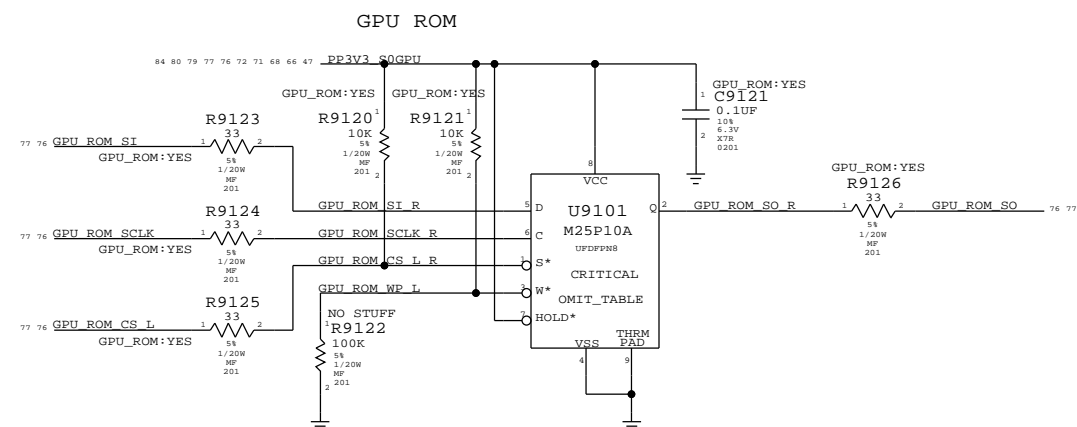
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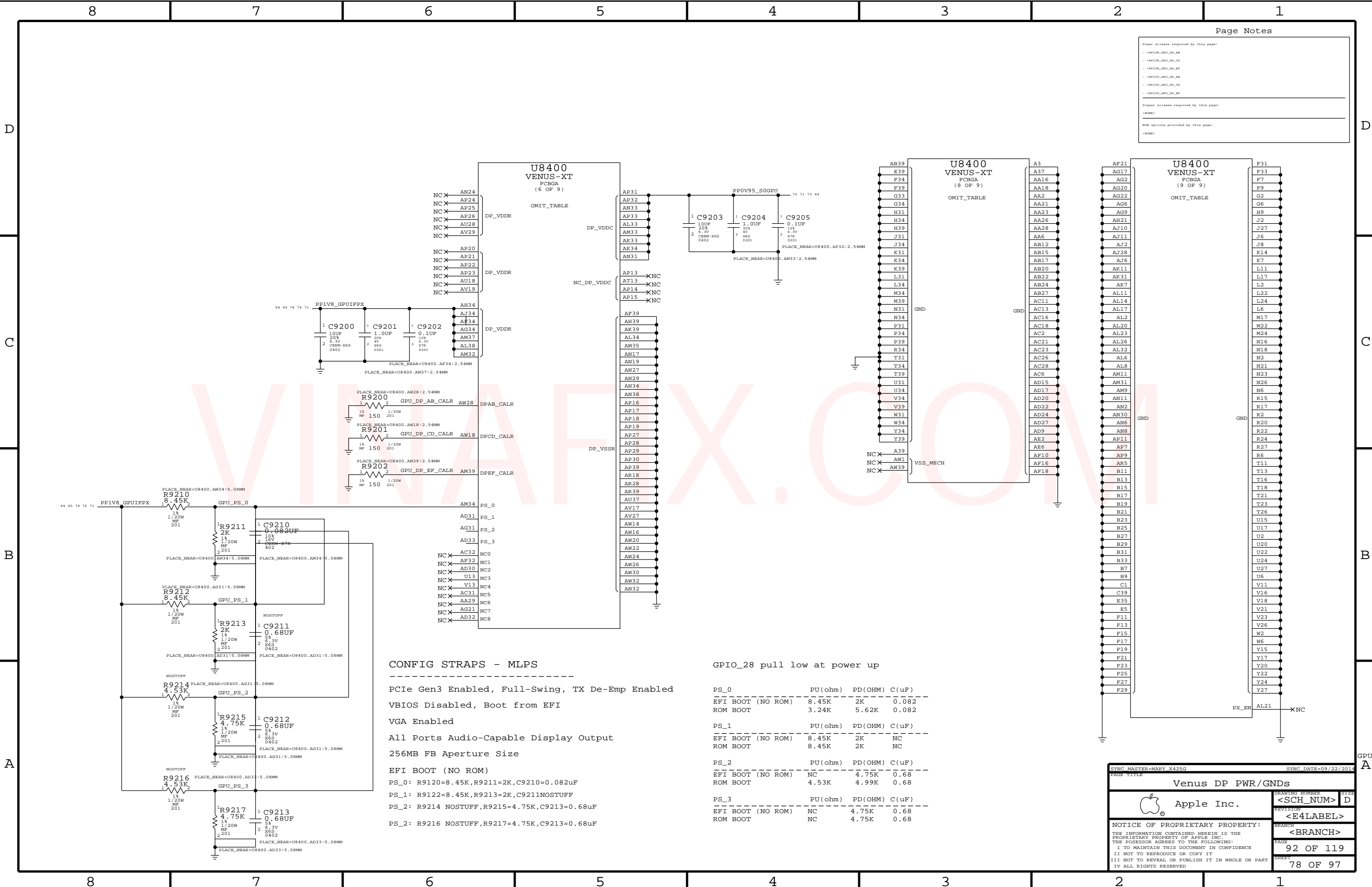




GPU GPIO TABLE									
		Native Func		GPIOs					
80	77	76	GFX VDDCI ALT_V	GPIO	==	GFX VDDCI ALT_V			76 77 80
	77	76	NC GPU GPIO 1	GPIO	==	NC GPU GPIO 1	MAKE_BASE=TRUE		76 77
	77	76	NC GPU GPIO 2	GPIO	==	NC GPU GPIO 2	MAKE_BASE=TRUE NO_TEST=TRUE		76 77
	77	76	GPU GFX_FWR_LEVEL_R_L	GPIO	==	GPU GFX_FWR_LEVEL_R_L	MAKE_BASE=TRUE NO_TEST=TRUE		76 77
	77	76	GFXIMVP_VR_ICCMA_X_WARN_L	GPIO	==	GFXIMVP_VR_ICCMA_X_WARN_L	MAKE_BASE=TRUE		76 77 79
	82	77	EG_BKLT_EN	GPIO	==	EG_BKLT_EN	MAKE_BASE=TRUE		76 77 82
	77	76	GPU_ROM_SO	GPIO	==	GPU_ROM_SO	MAKE_BASE=TRUE		76 77
	77	76	GPU_ROM_SI	GPIO	==	GPU_ROM_SI	MAKE_BASE=TRUE		76 77
	77	76	GPU_ROM_SCLK	GPIO	==	GPU_ROM_SCLK	MAKE_BASE=TRUE		76 77
	79	77	GPU_VCORE_VID4	GPIO	==	GPU_VCORE_VID4	MAKE_BASE=TRUE		76 77 79
	79	77	GPU_VCORE_VID5	GPIO	==	GPU_VCORE_VID5	MAKE_BASE=TRUE		76 77 79
	79	77	GPU_VCORE_VID0	GPIO	==	GPU_VCORE_VID0	MAKE_BASE=TRUE		76 77 79
	82	77	DP_TBTSNK1_HPD_EG	GPIO	==	DP_TBTSNK1_HPD_EG	MAKE_BASE=TRUE		76 77 82
	79	77	GPU_VCORE_VID1	GPIO	==	GPU_VCORE_VID1	MAKE_BASE=TRUE		76 77 79
		Native Func		GPIOs					
	79	77	GPU_VCORE_VID2	GPIO	==	GPU_VCORE_VID2	MAKE_BASE=TRUE		76 77 79
	77	76	GFX_SELF_THROTTLE_R	GPIO	==	GFX_SELF_THROTTLE_R	MAKE_BASE=TRUE		76 77
	82	77	HDMI_EG_HPD	GPIO	==	HDMI_EG_HPD	MAKE_BASE=TRUE		76 77 82
	77	76	GPU_GFX_OVERTEMP_R	GPIO	==	GPU_GFX_OVERTEMP_R	MAKE_BASE=TRUE		76 77
	79	77	GPU_VCORE_VID3	GPIO	==	GPU_VCORE_VID3	MAKE_BASE=TRUE		76 77 79
	77	76	FBVDD_ALTVO	GPIO	==	FBVDD_ALTVO	MAKE_BASE=TRUE		73 76 77
	77	76	GPU_ROM_CS_L	GPIO	==	GPU_ROM_CS_L	MAKE_BASE=TRUE		76 77
	77	76	TP_CLKRBO_L	GPIO	==	TP_CLKRBO_L	MAKE_BASE=TRUE		76 77
	77	76	NC_GPU_GENERICA	GPIO	==	NC_GPU_GENERICA	MAKE_BASE=TRUE NO_TEST=TRUE		76 77
	77	76	NC_GPU_GENERICB	GPIO	==	NC_GPU_GENERICB	MAKE_BASE=TRUE NO_TEST=TRUE		76 77
	77	76	GPU_VCORE_PSI_L	GPIO	==	GPU_VCORE_PSI_L	MAKE_BASE=TRUE		76 77
	79	77	GFXIMVP_DPSLP_EN_R	GPIO	==	GFXIMVP_DPSLP_EN_R	MAKE_BASE=TRUE		76 77 79
	77	76	NC_DP_EXTB_CA_DET_EG	GPIO	==	NC_DP_EXTB_CA_DET_EG	MAKE_BASE=TRUE NO_TEST=TRUE		76 77
	77	76	NC_DP_EXTB_CA_DET_EG	GPIO	==	NC_DP_EXTB_CA_DET_EG	MAKE_BASE=TRUE NO_TEST=TRUE		76 77
	77	76	NC_GPU_GPIO_33	GPIO	==	NC_GPU_GPIO_33	MAKE_BASE=TRUE NO_TEST=TRUE		76 77
	82	77	DP_INT_EG_HPD	GPIO	==	DP_INT_EG_HPD	MAKE_BASE=TRUE		76 77 82
	77	76	NC_GPU_GPIO_35	GPIO	==	NC_GPU_GPIO_35	MAKE_BASE=TRUE		76 77
	82	77	DP_TBTSNK0_HPD_EG	GPIO	==	DP_TBTSNK0_HPD_EG	MAKE_BASE=TRUE		76 77 82



SYNC MASTER=MARY X425G		SYNC DATE=11/07/2014	
PAGE 11111			
Venus GPIOs & STRAPS			
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Page Notes	
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F34	F34	AA16	F7
F39	F39	AA18	F9
G33	G33	AA22	G2
H31	H31	AA23	G6
H34	H34	AA26	H9
H39	H39	AA28	J2
J31	J31	AA6	J27
J34	J34	AB12	J6
K31	K31	AB15	J8
K34	K34	AB17	K14
K39	K39	AB20	K7
L31	L31	AB22	L11
L34	L34	AB24	L17
M34	M34	AB27	L2
M39	M39	AC11	L22
N31	N31	AC13	L24
N34	N34	AC16	L6
P31	P31	AC18	M17
P34	P34	AC2	M22
P39	P39	AC21	M24
R34	R34	AC23	N16
T31	T31	AC26	N18
T34	T34	AC28	N2
T39	T39	AC6	N21
U31	U31	AD15	N23
U34	U34	AD17	N26
V34	V34	AD20	N6
V39	V39	AD22	R15
W31	W31	AD24	R17
W34	W34	AD27	R2
Y34	Y34	AD9	R20
Y39	Y39	AE2	R22
NCX	AW1	AE6	R24
NCX	AW39	AF10	R27
NCX	AW39	AF16	R6
		AF18	T11
			T13
			T16
			T18
			T21
			T23
			T26
			U15
			U17
			U2
			U20
			U22
			U24
			U27
			U6
			V11
			V16
			V39
			E35
			E5
			F11
			F13
			F15
			F17
			F19
			F21
			F23
			F25
			F27
			F29
			PX_EN
			AL21
			NC

CONFIG STRAPS - MLPS

-----

PCIe Gen3 Enabled, Full-Swing, TX De-Emp Enabled

VBIOS Disabled, Boot from EFI

VGA Enabled

All Ports Audio-Capable Display Output

256MB FB Aperture Size

EFI BOOT (NO ROM)

PS\_0: R9120=8.45K,R9211=2K,C9210=0.082uF

PS\_1: R9122=8.45K,R9213=2K,C9211NOSTUFF

PS\_2: R9214 NOSTUFF,R9215=4.75K,C9213=0.68uF

PS\_2: R9216 NOSTUFF,R9217=4.75K,C9213=0.68uF

GPIO_28 pull low at power up			
	PU(ohm)	PD(OHM)	C(uF)
PS_0			
EFI BOOT (NO ROM)	8.45K	2K	0.082
ROM BOOT	3.24K	5.62K	0.082
PS_1			
EFI BOOT (NO ROM)	8.45K	2K	NC
ROM BOOT	8.45K	2K	NC
PS_2			
EFI BOOT (NO ROM)	NC	4.75K	0.68
ROM BOOT	4.53K	4.99K	0.68
PS_3			
EFI BOOT (NO ROM)	NC	4.75K	0.68
ROM BOOT	NC	4.75K	0.68

SYNC MASTER=MARY X425G

SYNC DATE=09/22/2014

PAGE TITLE

Venus DP PWR/GNDs

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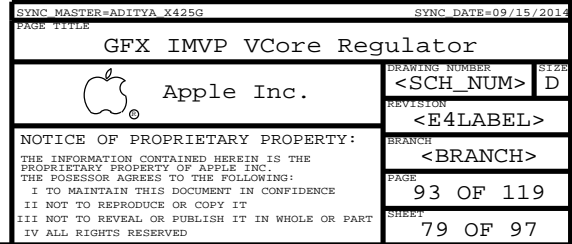
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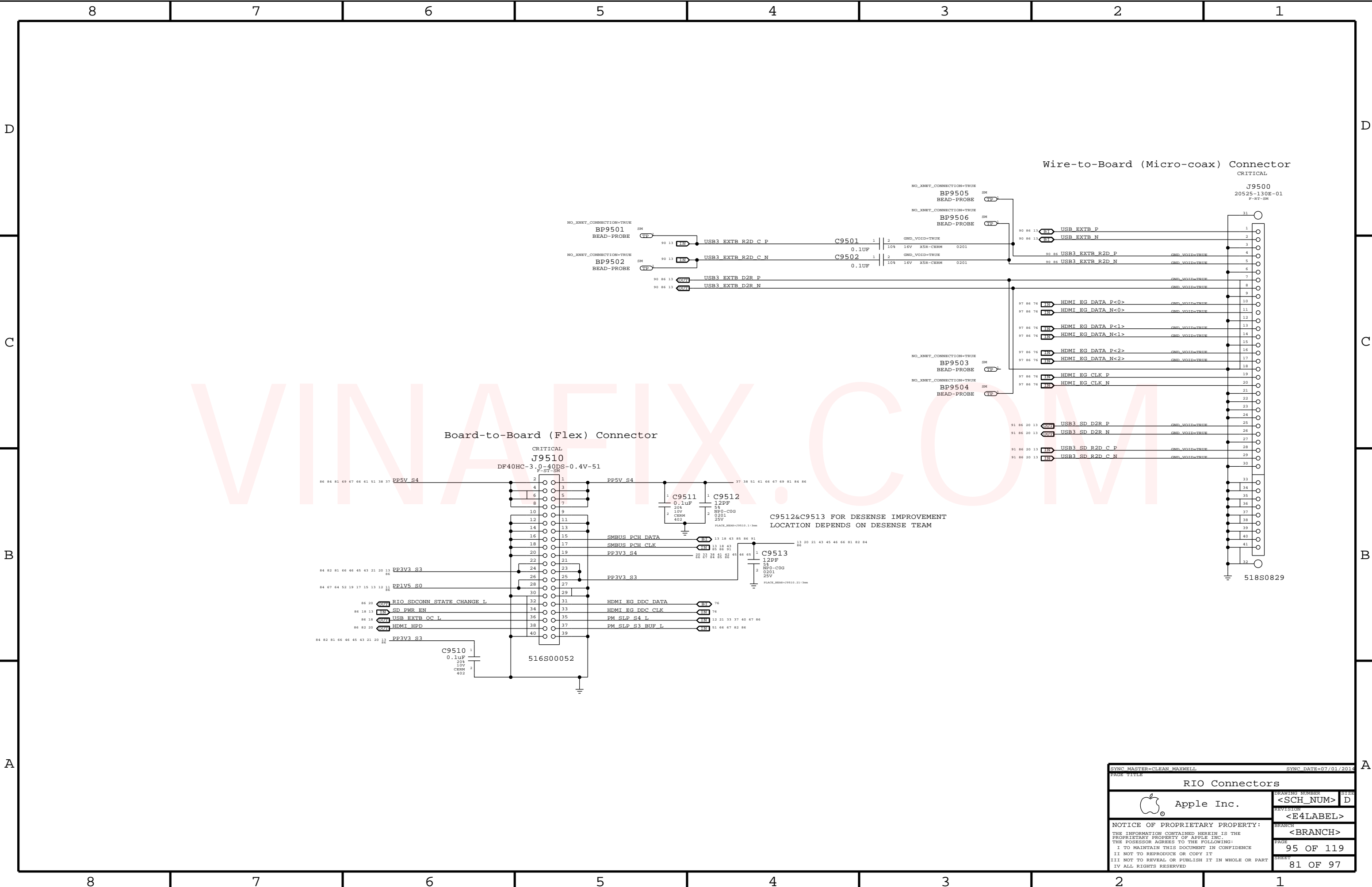
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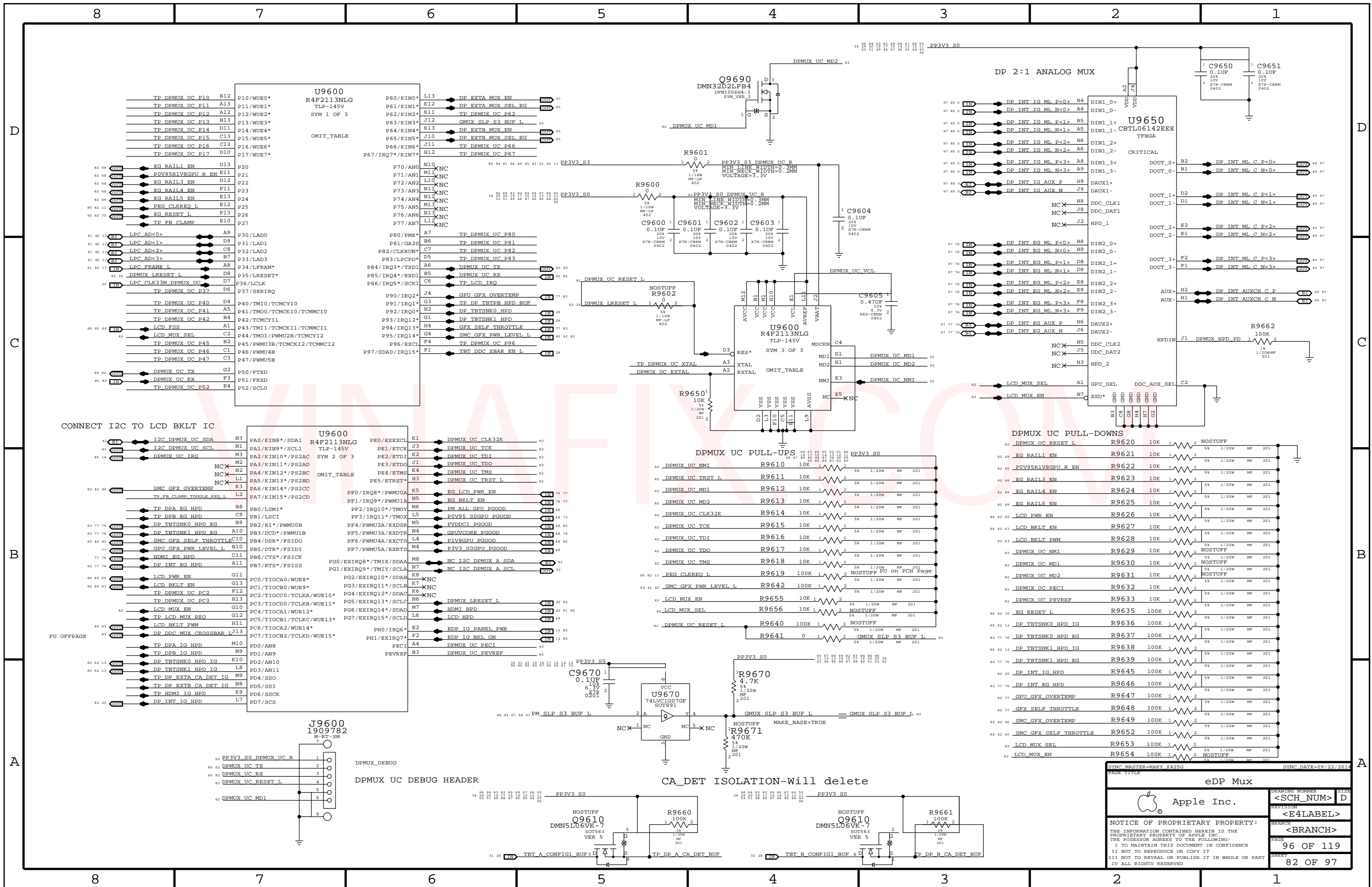


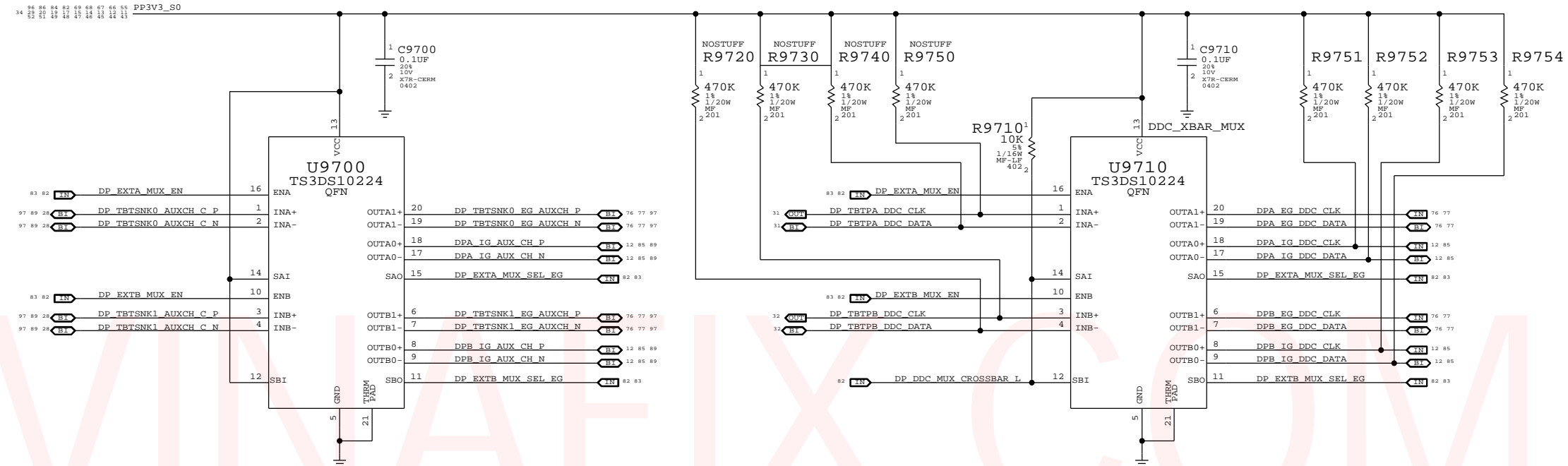






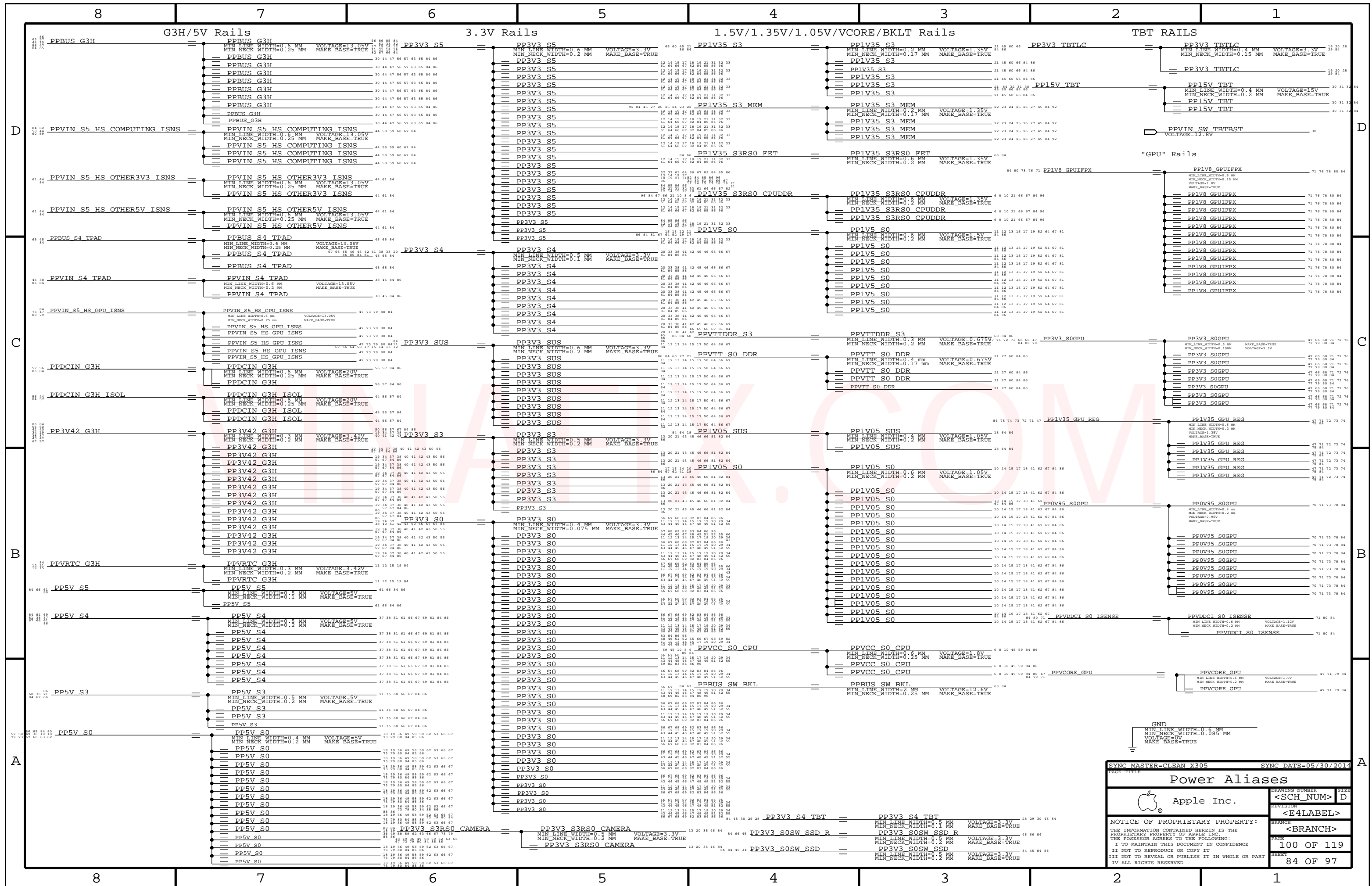






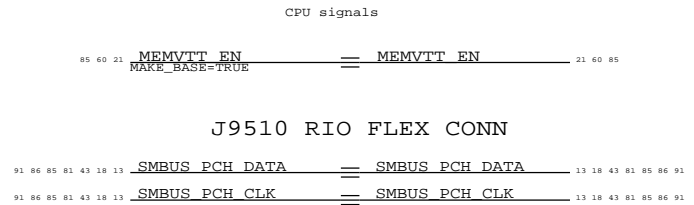
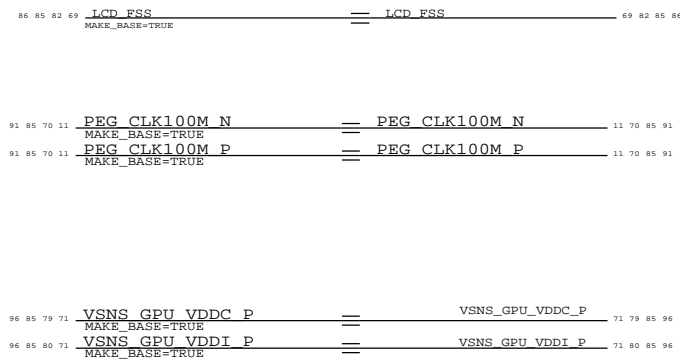
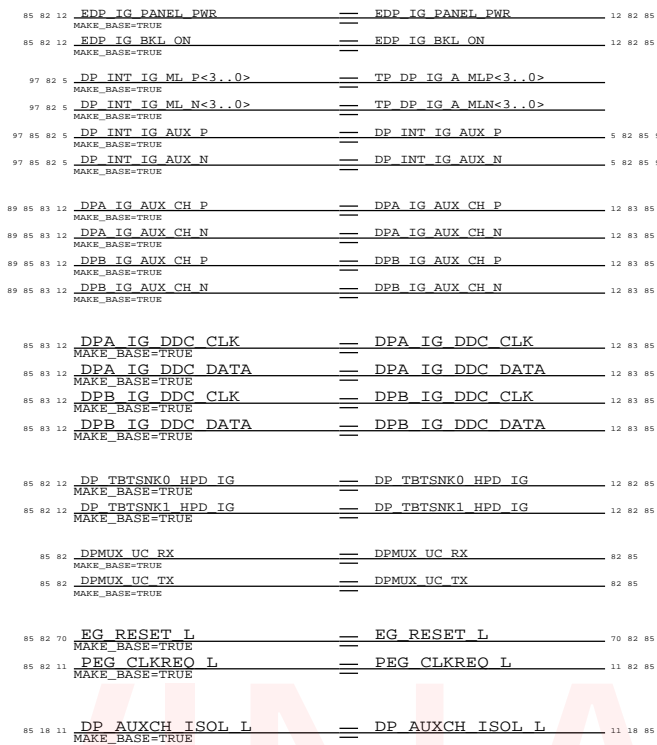
## MUX TRUTH TABLE

SAI / SBI	SAO	SBO	INA	INB
0	0	0	OUTB0	OUTA0
0	0	1	OUTB1	OUTA0
0	1	0	OUTB0	OUTA1
0	1	1	OUTB1	OUTA1
1	0	0	OUTA0	OUTB0
1	0	1	OUTA0	OUTB1
1	1	0	OUTA1	OUTB0
1	1	1	OUTA1	OUTB1

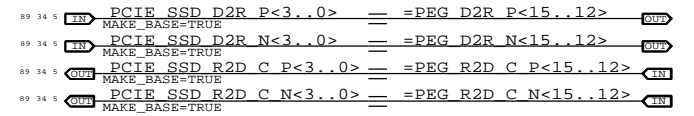




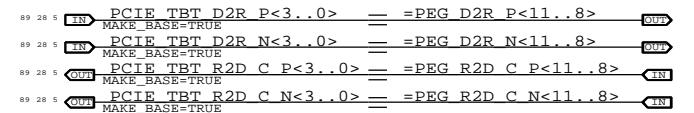
## Display Aliases



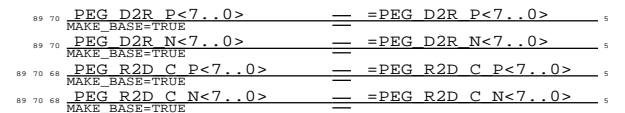
## SSD Signals Through PEG



## Thunderbolt Signals Through PEG

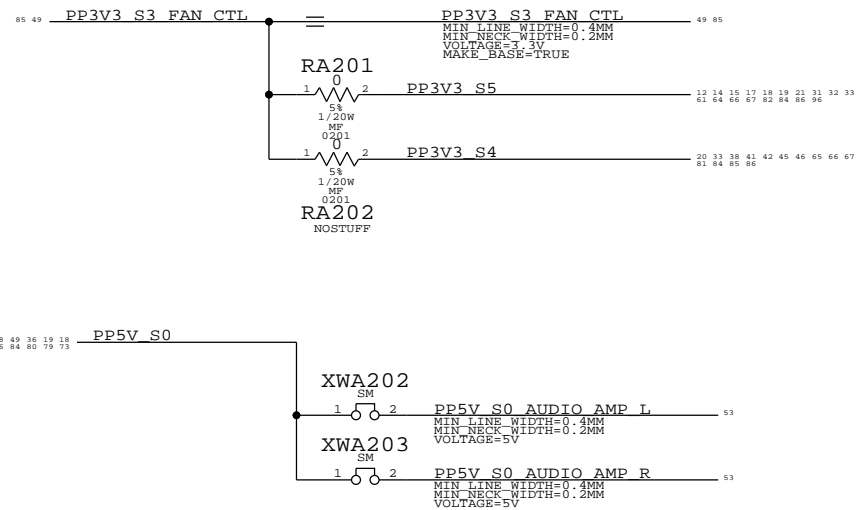
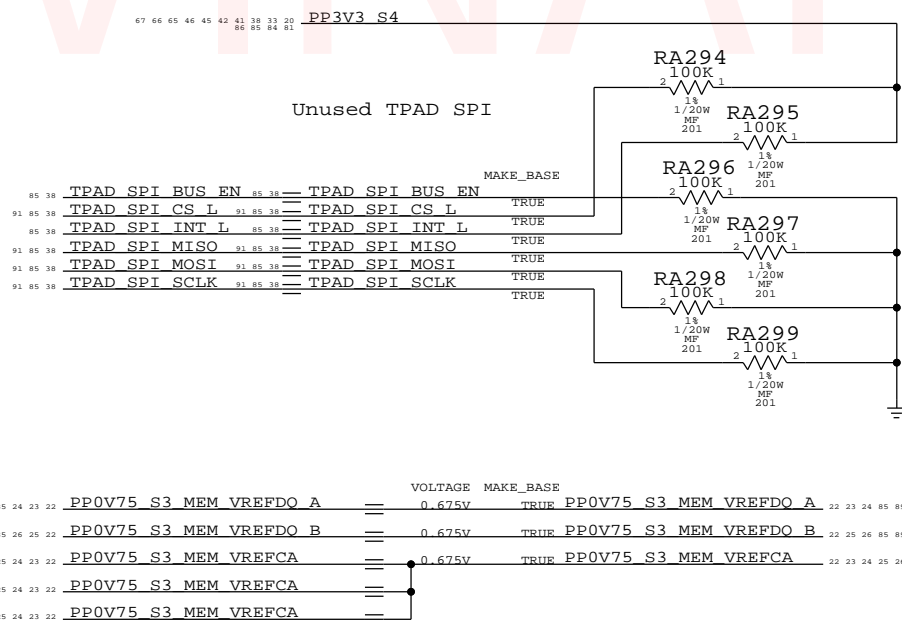


GUP PEG Lanes

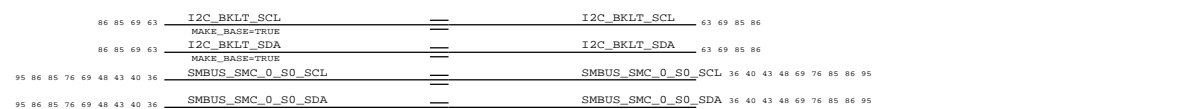


Unused PCH PCIe Lanes

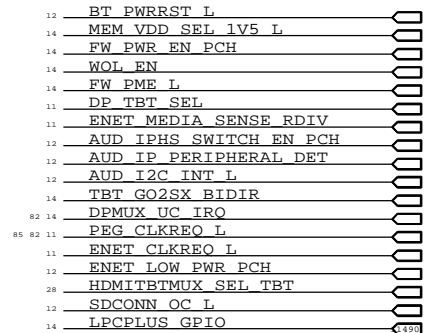
	MAKE_BASE	NO_TEST	
13	<u>NC PCIE SSD D2RP&lt;3..0&gt;</u>	TRUE	==PCIE SSD D2R P<3..0>
	<u>NC PCIE SSD D2RN&lt;3..0&gt;</u>	TRUE	==PCIE SSD D2R N<3..0>
13	<u>NC PCIE SSD R2D CP&lt;3..0&gt;</u>	TRUE	==PCIE SSD R2D C P<3..0>
13	<u>NC PCIE SSD R2D CN&lt;3..0&gt;</u>	TRUE	==PCIE SSD R2D C N<3..0>




## EDP CABLE



Unused signals



SYNCH MASTER=J15 MLB		SYNCH DATE=10/31/2012	
PAGE TITLE			
Signal Aliases			
	Apple Inc.	DRAWING NUMBER	SIZE
		<SCH_NUM>	
		REVISION	
		<E4LABEL>	
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		SHEET	85 OF 97



# Functional Test Points

FUNC_TEST J3501 - airport	
TRUE AP CLKREQ O L	33
TRUE AP RESET CONN L	33
TRUE PCIE AP D2R PI N	91
TRUE PCIE AP D2R PI P	91
TRUE PCIE AP R2D N	33 91
TRUE PCIE AP R2D P	33 91
TRUE PCIE CLK100M AP CONN N	33 91
TRUE PCIE CLK100M AP CONN P	33 91
TRUE PCIE WAKE L	12 33 35 91
TRUE PP3V3 S3RS4 BT F	33
TRUE PP3V3 WLAN	33 41
TRUE USB BT CONN N	33 90
TRUE USB BT CONN P	33 90
TRUE WIFI EVENT L	33 40 41
TRUE GND	4X

J4002 - Camera	
TRUE MIPI CLK CONN N	36 94
TRUE MIPI CLK CONN P	36 94
TRUE CAM SENSOR WAKE L CONN	36
TRUE MIPI DATA CONN N	36 94
TRUE MIPI DATA CONN P	36 94
TRUE SMBUS SMC 0 S0 SDA	36 40 43 48 69 76 85 86 95
TRUE SMBUS SMC 0 S0 SCL	36 40 43 48 69 76 85 86 95
TRUE I2C CAM SCK	35 36
TRUE I2C CAM SDA	35 36
TRUE PP5V S3RS0 ALSCAM F	36
TRUE GND	

J9500 - rio coax	
TRUE HDMI EG CLK N	76 81 97
TRUE HDMI EG CLK P	76 81 97
TRUE HDMI EG DATA N<0>	76 81 97
TRUE HDMI EG DATA N<1>	76 81 97
TRUE HDMI EG DATA N<2>	76 81 97
TRUE HDMI EG DATA P<0>	76 81 97
TRUE HDMI EG DATA P<1>	76 81 97
TRUE HDMI EG DATA P<2>	76 81 97

TRUE USB3 SD D2R N	13 20 81 91
TRUE USB3 SD D2R P	13 20 81 91
TRUE USB3 SD R2D C N	13 20 81 91
TRUE USB3 SD R2D C P	13 20 81 91
TRUE USB3 EXTB D2R N	13 81 90
TRUE USB3 EXTB D2R P	13 81 90
TRUE USB3 EXTB R2D N	81 90
TRUE USB3 EXTB R2D P	81 90
TRUE USB EXTB N	13 81 90
TRUE USB EXTB P	13 81 90
TRUE GND	19X

J9510 - rio flex	
TRUE SD PWR EN	13 18 81
TRUE HDMI DDC CLK	
TRUE HDMI DDC DATA	
TRUE HDMI HPD	20 81 82
TRUE SMBUS PCH CLK	13 18 43 81 85 91
TRUE SMBUS PCH DATA	13 18 43 81 85 91
TRUE PM SLP S3 BUF L	61 66 67 81 82
TRUE PM SLP S4 L	12 21 33 37 40 67 81
TRUE PP3V3 S3	3X 13 20 21 43 45 46 66 81 82
TRUE PP3V3 S4	20 33 38 41 42 45 46 65 66 67
TRUE PP5V S4	5X 13 38 51 61 66 67 69 81 84
TRUE RIO SDCONN STATE CHANGE L	20 81
TRUE USB EXTB OC L	18 81
TRUE GND	10X

J5150 - hall effect	
TRUE PP3V42 G3H	19 34 37 38 40 41 42 43 50 56
TRUE SMC LID R	42
TRUE GND	

J6050 - left fan	
TRUE FAN LT PWM	49
TRUE FAN LT TACH	49
TRUE PP5V S0	3X 18 19 36 49 58 59 62 63 66
TRUE GND	5X

J6060 - right fan	
TRUE FAN RT PWM	49
TRUE FAN RT TACH	49
TRUE PP5V S0	3X 18 19 36 49 58 59 62 63 66
TRUE GND	5X

FUNC_TEST J6100 - spi	
TRUE PP3V42 G3H	19 34 37 38 40 41 42 43 50 56
TRUE SMC RESET L	40 41 50 57
TRUE SMC TCK	40 41 50
TRUE SMC TMS	40 41 50
TRUE SPIROM USE MLB	14 50
TRUE GND	2X

J4801 - ipd flex	
TRUE USB TPAD N	13 38 90
TRUE USB TPAD P	13 38 90
TRUE IOXP2 INT L	38
TRUE I2C IOXP SCL	38
TRUE I2C IOXP SDA	38
TRUE SMC PME S4 WAKE L	13 38 40 42
TRUE TPAD ACTUATOR THRMTTRIP L	38 65
TRUE TPAD VBUS EN	38 67
TRUE SMBUS SMC 2 S3 SCL	38 40 43 95
TRUE SMBUS SMC 2 S3 SDA	38 40 43 95
TRUE SMC LID	38 40 41 42
TRUE SMC ACTUATOR EN L	38 40
TRUE PPVIN S4 TPAD	4X 38 45 84
TRUE GND ACTUATOR	4X 38
TRUE PP3V3 S4	20 33 38 41 42 45 46 65 66 67
TRUE PP5V S4	81 84 85 86
TRUE GND	2X

J4813 - keyboard	
TRUE PP3V3 S4	20 33 38 41 42 45 46 65 66 67
TRUE PP3V42 G3H	19 34 37 38 40 41 42 43 50 56
TRUE WS CONTROL KBD	38
TRUE WS KBD1	38
TRUE WS KBD10	38
TRUE WS KBD11	38
TRUE WS KBD12	38
TRUE WS KBD13	38
TRUE WS KBD14	38
TRUE WS KBD15 CAP	38
TRUE WS KBD16 NUM	38
TRUE WS KBD17	38
TRUE WS KBD18	38
TRUE WS KBD19	38
TRUE WS KBD20	38
TRUE WS KBD21	38
TRUE WS KBD22	38
TRUE WS KBD23	38
TRUE WS KBD3	38
TRUE WS KBD4	38
TRUE WS KBD5	38
TRUE WS KBD6	38
TRUE WS KBD7	38
TRUE WS KBD8	38
TRUE WS KBD9	38
TRUE WS KBD ONOFF L	38
TRUE WS LEFT OPTION KBD	38
TRUE WS LEFT SHIFT KBD	38
TRUE GND	2X

J4915 - kbd bklt	
TRUE KBD BKLT RETURN1	2X 39 63
TRUE KBD BKLT RETURN2	2X 39 63
TRUE PPVOUT S0 KBD BKLT	39 63
TRUE GND	4X

J6601 - mic	
TRUE DMIC CLK3	52 55
TRUE PP3V3 S0	66 67 68 69 72 73 74 75 76 77 78 79 80 81 82 83 84 85 86 87 88 89 90 91 92 93 94
TRUE DMIC SDA2	55
TRUE DMIC SDA3	52 55
TRUE GND	

J6602 - L speaker	
TRUE SPKRCONN L ID	52 55
TRUE SPKRCONN L OUT N	53 55 96
TRUE SPKRCONN L OUT P	53 55 96
TRUE SPKRCONN SL OUT N	53 55 96
TRUE SPKRCONN SL OUT P	53 55 96
TRUE GND	

J6603 - R speaker	
TRUE SPKRCONN R ID	52 55
TRUE SPKRCONN R OUT N	53 55 96
TRUE SPKRCONN R OUT P	53 55 96
TRUE SPKRCONN SR OUT N	53 55 96
TRUE SPKRCONN SR OUT P	53 55 96
TRUE GND	

J7000 - DC PWR	
TRUE ADAPTER SENSE	56
TRUE PP20V DCIN FUSE	2X 16
TRUE GND	2X

J7050 - battery	
TRUE PPVBAT G3H CONN	8X 16 57
TRUE SMBUS SMC 5 G3 SCL	40 43 56 57 95
TRUE SMBUS SMC 5 G3 SDA	40 43 56 57 95
TRUE SYS DETECT L	56
TRUE GND	8X

J8300 - eDP	
TRUE DP INT AUX N	69 97
TRUE DP INT AUX P	69 97
TRUE DP INT ML N<0>	69 97
TRUE DP INT ML N<1>	69 97
TRUE DP INT ML N<2>	69 97
TRUE DP INT ML N<3>	69 97
TRUE DP INT ML P<0>	69 97
TRUE DP INT ML P<1>	69 97
TRUE DP INT ML P<2>	69 97
TRUE DP INT ML P<3>	69 97
TRUE LCD FSS	69 82 85
TRUE LCD HPD CONN	69
TRUE LCD BKLT PWM R	63 69
TRUE SMBUS SMC 0 S0 SDA	36 40 43 48 69 76 85 86 95
TRUE SMBUS SMC 0 S0 SCL	36 40 43 48 69 76 85 86 95
TRUE I2C BKLT SDA	63 69 85
TRUE I2C BKLT SCL	63 69 85
TRUE PP5VR3V3 SW LCD	3X 69
TRUE PPVOUT S0 LCDBKLT	63 69
TRUE GND	16X

Power Rails	
TRUE PM SLP S3 L	12 21 40 67
TRUE PPVTT S0 DDR	21 27 60 84
TRUE PP3V3 S0	66 67 68 69 72 73 74 75 76 77 78 79 80 81 82 83 84 86 96 34
TRUE PP3V3 S3	12 13 14 15 17 18 20 28 34
TRUE PP3V3 S5	86
TRUE PP3V3 S5 AVREF SMC	22 23 24 25 26 27 28 29 30 31 32 33
TRUE PP3V42 G3H	40 41
TRUE PP5V S0	19 34 37 38 40 41 42 43 50 56
TRUE PP5V S3	19 34 37 38 40 41 42 43 50 56
TRUE PP5V S5	21 36 60 66 67 84
TRUE PPBUS G3H	61 66 84
TRUE PPDCIN G3H	56 57 84
TRUE PPVCC S0 CPU	6 8 10 45 59 84
TRUE PPVTDDR S3	40 84
TRUE PP3V3 S0SW SSD	34 45 84
TRUE PP1V5 S0	21 13 15 17 19 52 64 67 81
TRUE PP1V35 S3	21 45 60 66 84

FUNC_TEST XDP	
TRUE XDP CPU TCK	6 18 89
TRUE XDP PCH TCK	11 18
TRUE XDP CPU TDI	6 18 89
TRUE XDP CPU TDO	6 18 89
TRUE XDP CPUPCH TRST L	6 18 89
TRUE XDP CPU TMS	6 18 89
TRUE XDP PCH TMS	11 18
TRUE XDP PCH TDI	11 18
TRUE XDP PCH TDO	11 18
TRUE XDP CPU FREQ L	6 18 89
TRUE XDP CPU PRDY L	6 18 89
TRUE PM RSMRST L	12 67 91
TRUE PM PCH PWROK	12 19 91
TRUE PM SYSRST L	12 19 40 91
TRUE CPU CFG<3>	6 18 89
TRUE PP1V05 S0	10 14 15 17 18 41 62 67 84
TRUE GND	2X GND

FUNC_TEST Power Sequence	
TRUE SMC ONOFF L	38 40 41
TRUE PM DSW PWRGD	12 40 91
TRUE ALL SYS PWRGD	18 19 40 58 67
TRUE PM PCH SYS PWROK	12 18 19 40 91
TRUE PLT RESET L	12 18 20 21
TRUE LCD PWR EN	69 82
TRUE LCD BKLT EN	63 82

FUNC_TEST GPU_VENUS JTAG	
TRUE GPU JTAG TCK	76 77
TRUE GPU JTAG TDI	76 77
TRUE GPU JTAG TDO	76 77
TRUE GPU JTAG TMS	76 77
TRUE GPU JTAG TRST L	76 77
TRUE GPU PWRGOOD	76 77

SYNC MASTER=J15 MLB		SYNC DATE=10/31/2012	
PAGE TITLE			
Functional Test Points		DRAWING NUMBER	SIZE
		<SCH_NUM>	D
		REVISION	
		<E4LABEL>	
		BRANCH	
		<BRANCH>	
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8	7	6	5	4	3	2	1						
NC NO_TESTS													
PCH				Thunderbolt		PLACEABLE BEAD-PROBES FOR TBT							
NO_TEST MAKE_BASE				NO_TEST MAKE_BASE									
87 13	NC USB3 SPARE D2RN	==	TRUE	TRUE	NC USB3 SPARE D2RN	13 87	87 28	NC TBT XTAL25OUT	==	TRUE	TRUE	NC TBT XTAL25OUT	28 87
87 13	NC USB3 SPARE D2RP	==	TRUE	TRUE	NC USB3 SPARE D2RP	13 87							
87 13	NC USB3 SPARE R2D CN	==	TRUE	TRUE	NC USB3 SPARE R2D CN	13 87							
87 13	NC USB3 SPARE R2D CP	==	TRUE	TRUE	NC USB3 SPARE R2D CP	13 87							
90 87 13	NC USB3 EXTC D2RN	==	TRUE	TRUE	NC USB3 EXTC D2RN	13 87 90							
90 87 13	NC USB3 EXTC D2RP	==	TRUE	TRUE	NC USB3 EXTC D2RP	13 87 90							
90 87 13	NC USB3 EXTC R2D CN	==	TRUE	TRUE	NC USB3 EXTC R2D CN	13 87 90							
90 87 13	NC USB3 EXTC R2D CP	==	TRUE	TRUE	NC USB3 EXTC R2D CP	13 87 90							
90 87 13	NC USB3 EXTD D2RN	==	TRUE	TRUE	NC USB3 EXTD D2RN	13 87 90							
90 87 13	NC USB3 EXTD D2RP	==	TRUE	TRUE	NC USB3 EXTD D2RP	13 87 90							
90 87 13	NC USB3 EXTD R2D CN	==	TRUE	TRUE	NC USB3 EXTD R2D CN	13 87 90							
90 87 13	NC USB3 EXTD R2D CP	==	TRUE	TRUE	NC USB3 EXTD R2D CP	13 87 90							
87	NC PCIE ENET D2RN	==	TRUE	TRUE	NC PCIE ENET D2RN	87							
87	NC PCIE ENET D2RP	==	TRUE	TRUE	NC PCIE ENET D2RP	87							
87	NC PCIE ENET R2D CN	==	TRUE	TRUE	NC PCIE ENET R2D CN	87							
87	NC PCIE ENET R2D CP	==	TRUE	TRUE	NC PCIE ENET R2D CP	87							
87 12	NC DP IG D AUXCHN	==	TRUE	TRUE	NC DP IG D AUXCHN	12 87							
87 12	NC DP IG D AUXCHP	==	TRUE	TRUE	NC DP IG D AUXCHP	12 87							
90 87 11	NC SATA A D2RN	==	TRUE	TRUE	NC SATA A D2RN	11 87 90							
90 87 11	NC SATA A D2RP	==	TRUE	TRUE	NC SATA A D2RP	11 87 90							
90 87 11	NC SATA A R2D CN	==	TRUE	TRUE	NC SATA A R2D CN	11 87 90							
90 87 11	NC SATA A R2D CP	==	TRUE	TRUE	NC SATA A R2D CP	11 87 90							
90 87 11	NC SATA B D2RN	==	TRUE	TRUE	NC SATA B D2RN	11 87 90							
90 87 11	NC SATA B D2RP	==	TRUE	TRUE	NC SATA B D2RP	11 87 90							
90 87 11	NC SATA B R2D CN	==	TRUE	TRUE	NC SATA B R2D CN	11 87 90							
90 87 11	NC SATA B R2D CP	==	TRUE	TRUE	NC SATA B R2D CP	11 87 90							
90 87 11	NC SATA ODD D2RN	==	TRUE	TRUE	NC SATA ODD D2RN	11 87 87							
90 87 11	NC SATA ODD D2RP	==	TRUE	TRUE	NC SATA ODD D2RP	11 87 87							
90 87 11	NC SATA ODD R2D CN	==	TRUE	TRUE	NC SATA ODD R2D CN	11 87 87							
90 87 11	NC SATA ODD R2D CP	==	TRUE	TRUE	NC SATA ODD R2D CP	11 87 87							
90 87 11	NC SATA D D2RN	==	TRUE	TRUE	NC SATA D D2RN	11 87 87							
90 87 11	NC SATA D D2RP	==	TRUE	TRUE	NC SATA D D2RP	11 87							
90 87 11	NC SATA D R2D CN	==	TRUE	TRUE	NC SATA D R2D CN	11 87							
90 87 11	NC SATA D R2D CP	==	TRUE	TRUE	NC SATA D R2D CP	11 87							
90 87 11	NC SATA F D2RN	==	TRUE	TRUE	NC SATA F D2RN	11 87							
90 87 11	NC SATA F D2RP	==	TRUE	TRUE	NC SATA F D2RP	11 87							
90 87 11	NC SATA F R2D CN	==	TRUE	TRUE	NC SATA F R2D CN	11 87							
90 87 11	NC SATA F R2D CP	==	TRUE	TRUE	NC SATA F R2D CP	11 87							
90 87 13	NC USB EXTCN	==	TRUE	TRUE	NC USB EXTCN	13 87 90							
90 87 13	NC USB EXTCP	==	TRUE	TRUE	NC USB EXTCP	13 87 90							
90 87 13	NC USB SDN	==	TRUE	TRUE	NC USB SDN	13 87 90							
90 87 13	NC USB SDP	==	TRUE	TRUE	NC USB SDP	13 87 90							
87 13	NC USB WLANN	==	TRUE	TRUE	NC USB WLANN	13 87							
87 13	NC USB WLAMP	==	TRUE	TRUE	NC USB WLAMP	13 87							
90 87 13	NC USB 6N	==	TRUE	TRUE	NC USB 6N	13 87 90							
90 87 13	NC USB 6P	==	TRUE	TRUE	NC USB 6P	13 87 90							
90 87 13	NC USB 7N	==	TRUE	TRUE	NC USB 7N	13 87 90							
90 87 13	NC USB 7P	==	TRUE	TRUE	NC USB 7P	13 87 90							
90 87 13	NC USB EXTDN	==	TRUE	TRUE	NC USB EXTDN	13 87 90							
90 87 13	NC USB EXTDP	==	TRUE	TRUE	NC USB EXTDP	13 87 90							
87 13	NC USB PSOCN	==	TRUE	TRUE	NC USB PSOCN	13 87							
87 13	NC USB PSOCP	==	TRUE	TRUE	NC USB PSOCP	13 87							
90 87 13	NC USB IRN	==	TRUE	TRUE	NC USB IRN	13 87 90							
90 87 13	NC USB IRP	==	TRUE	TRUE	NC USB IRP	13 87 90							
89 87 11	NC ITPXDP CLK100MN	==	TRUE	TRUE	NC ITPXDP CLK100MN	11 87 89							
89 87 11	NC ITPXDP CLK100MP	==	TRUE	TRUE	NC ITPXDP CLK100MP	11 87 89							
87 12	NC PCI PME L	==	TRUE	TRUE	NC PCI PME L	12 87							
87 11	NC PCI CLK33M OUT3	==	TRUE	TRUE	NC PCI CLK33M OUT3	11 87							
87 11	NC HDA SDIN1	==	TRUE	TRUE	NC HDA SDIN1	11 87							
87 11	NC HDA SDIN2	==	TRUE	TRUE	NC HDA SDIN2	11 87							
87 11	NC HDA SDIN3	==	TRUE	TRUE	NC HDA SDIN3	11 87							
87 13	NC LPC DREQ0 L	==	TRUE	TRUE	NC LPC DREQ0 L	13 87							
87 13	NC CLINK CLK	==	TRUE	TRUE	NC CLINK CLK	13 87							
87 13	NC CLINK DATA	==	TRUE	TRUE	NC CLINK DATA	13 87							
87 13	NC CLINK RESET L	==	TRUE	TRUE	NC CLINK RESET L	13 87							
91 87 11	NC LPC CLK33M LPCPLUS R	==	TRUE	TRUE	NC LPC CLK33M LPCPLUS R	11 87 91							
87 12	NC EDP IG BKL PWM	==	TRUE	TRUE	NC EDP IG BKL PWM	12 87							
90 87	NC USB SMCN	==	TRUE	TRUE	NC USB SMCN	87 90							
90 87	NC USB SMCN	==	TRUE	TRUE	NC USB SMCN	87 90							
87	NC SMC INTERFACE 2	==	TRUE	TRUE	NC SMC INTERFACE 2	87							

8	7	6	5	4	3	2	1
X425G BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS							
BOARD LAYERS				BOARD AREAS		BOARD UNITS (MIL OR MM)	ALLEGRO VERSION
TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, ISL10, ISL11, BOTTOM				NO_TYPE, BGA, P65BGA		MM	16.2
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=45_OHM_SE	=45_OHM_SE	10 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP, BOTTOM	Y	0.095 MM	0.095 MM			
50_OHM_SE	*	Y	0.066 MM	0.066 MM	=STANDARD	=STANDARD	=STANDARD
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP, BOTTOM	Y	0.116 MM	0.116 MM			
45_OHM_SE	*	Y	0.083 MM	0.083 MM	=STANDARD	=STANDARD	=STANDARD
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP, BOTTOM	Y	0.145 MM	0.095 MM			
40_OHM_SE	*	Y	0.102 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
37_OHM_SE	TOP, BOTTOM	Y	0.165 MM	0.095 MM			
37_OHM_SE	*	Y	0.118 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP, BOTTOM	Y	0.265 MM	0.095 MM			
27P4_OHM_SE	*	Y	0.186 MM	0.1 MM	=STANDARD	=STANDARD	=STANDARD
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
72_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
72_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.105 MM	0.105 MM		0.120 MM	0.120 MM
72_OHM_DIFF	ISL2, ISL11	Y	0.105 MM	0.105 MM		0.120 MM	0.120 MM
72_OHM_DIFF	TOP, BOTTOM	Y	0.146 MM	0.146 MM		0.120 MM	0.120 MM
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
80_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.092 MM	0.092 MM		0.120 MM	0.120 MM
80_OHM_DIFF	ISL2, ISL11	Y	0.092 MM	0.092 MM		0.120 MM	0.120 MM
80_OHM_DIFF	TOP, BOTTOM	Y	0.125 MM	0.125 MM		0.155 MM	0.155 MM
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.080 MM	0.080 MM		0.120 MM	0.120 MM
85_OHM_DIFF	ISL2, ISL11	Y	0.080 MM	0.080 MM		0.120 MM	0.120 MM
85_OHM_DIFF	TOP, BOTTOM	Y	0.105 MM	0.105 MM		0.125 MM	0.125 MM
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.078 MM	0.078 MM		0.200 MM	0.200 MM
90_OHM_DIFF	ISL2, ISL11	Y	0.078 MM	0.078 MM		0.200 MM	0.200 MM
90_OHM_DIFF	TOP, BOTTOM	Y	0.101 MM	0.101 MM		0.180 MM	0.180 MM
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	P072_SPACE
*	*	P65BGA	P075_SPACE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	0.1 MM	?
BGA_P2MM	*	0.2 MM	?
P072_SPACE	*	0.071 MM	?
P075_SPACE	*	0.075 MM	?

Stackup-Defined Spacing Rules

Note: Outer dielectric is 0.058 mm nominal,  
Inner dielectric is 0.053 mm nominal.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	*	0.1 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1x_DIELECTRIC	TOP, BOTTOM	0.058 MM	?
1x_DIELECTRIC	ISL3, ISL4, ISL9, ISL10	0.053 MM	?
1x_DIELECTRIC	ISL2, ISL5, ISL6, ISL7, ISL8, ISL11	0.101 MM	?


PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
P65_BGA	*	Y	0.071MM	0.071MM		0.075MM	0.126MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
*	P65BGA	P65_BGA

SYNC MASTER=SIDLE J45

SYNC DATE=12/10/2012

PCB Rule Definitions

 Apple Inc.

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## CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL
CPU_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?	CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?
CPU_8MIL	*	8 MIL	?	CPU_VID	*	0.457 MM	?
CPU_COMP	*	20 MIL	?	CPU_VREF	*	12 MIL	?
CPU_ITP	*	=2:1_SPACING	?				
CPU_VCCSENSE	*	25 MIL	?				

Most CPU signals with impedance requirements are 50-ohm single-ended.  
Some signals require 27.4-ohm single-ended impedance.

SOURCE: IVB PLATFORM DG , Tables 205-207

## Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DMI_2SAME	*	=3X_DIELECTRIC	?	DMI_2SAME	TOP,BOTTOM	=4X_DIELECTRIC	?
DMI_TXRX	*	=6X_DIELECTRIC	?	DMI_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
DMICKLK2N2S	*	=6X_DIELECTRIC	?	DMICKLK2N2S	TOP,BOTTOM	=10X_DIELECTRIC	?
DMICKLK2S2N	*	=3X_DIELECTRIC	?	DMICKLK2S2N	TOP,BOTTOM	=6X_DIELECTRIC	?
DMICKLK2OTHER	*	=4X_DIELECTRIC	?	DMICKLK2OTHER	TOP,BOTTOM	=4X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DMI_*	=SAME	*	DMI_2SAME
DMI_N2S	DMI_S2N	*	DMI_TXRX
DMI_S2N	DMI_N2S	*	DMI_TXRX
CLK_DMI	DMI_N2S	*	DMICKLK2N2S
CLK_DMI	DMI_S2N	*	DMICKLK2S2N
CLK_DMI	*	*	DMICKLK2OTHER

## PEG - SSD &amp; TBT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PEG_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PEG_2SAME	*	=3X_DIELECTRIC	?	PEG_2SAME	TOP,BOTTOM	=4X_DIELECTRIC	?
PEG_TXRX	*	=6X_DIELECTRIC	?	PEG_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
PEG_2OTHER	*	=4X_DIELECTRIC	?	PEG_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?
PEG_2CLK	*	=7X_DIELECTRIC	?	PEG_2CLK	TOP,BOTTOM	=10X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PEG3_2SAME	*	=4X_DIELECTRIC	?	PEG3_2SAME	TOP,BOTTOM	=6X_DIELECTRIC	?
PEG3_TXRX	*	=8X_DIELECTRIC	?	PEG3_TXRX	TOP,BOTTOM	=12X_DIELECTRIC	?
PEG3_2OTHER	*	=5X_DIELECTRIC	?	PEG3_2OTHER	TOP,BOTTOM	=8X_DIELECTRIC	?
PEG3_2CLK	*	=8X_DIELECTRIC	?	PEG3_2CLK	TOP,BOTTOM	=12X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET	NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PEG_*	=SAME	*	PEG_2SAME	PEG3_*	=SAME	*	PEG3_2SAME
PEG_R2D	PEG_D2R	*	PEG_TXRX	PEG3_R2D	PEG3_D2R	*	PEG3_TXRX
PEG_*	*	*	PEG_2OTHER	PEG3_*	*	*	PEG3_2OTHER
PEG_*	CLK_*	*	PEG_2CLK	PEG3_*	CLK_*	*	PEG3_2CLK

## DIGITAL VIDEO SIGNAL CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP_2SAME	*	=3X_DIELECTRIC	?	DP_2SAME	TOP,BOTTOM	=4X_DIELECTRIC	?
DP_2OTHER	*	=4X_DIELECTRIC	?	DP_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?
HDMICKLK_2CLK	*	=7X_DIELECTRIC	?	HDMICKLK_2CLK	TOP,BOTTOM	=10X_DIELECTRIC	?
HDMICKLK_2DP	*	=6X_DIELECTRIC	?	HDMICKLK_2DP	TOP,BOTTOM	=6X_DIELECTRIC	?
HDMICKLK_2OTHER	*	=7X_DIELECTRIC	?	HDMICKLK_2OTHER	TOP,BOTTOM	=10X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DISPLAYPORT	=SAME	*	DP_2SAME
DISPLAYPORT	*	*	DP_2OTHER
HDMI_CLK	CLK_*	*	HDMICKLK_2CLK
HDMI_CLK	DISPLAYPORT	*	HDMICKLK_2DP
HDMI_CLK	*	*	HDMICKLK_2OTHER

DisplayPort/TMDs intra-pair matching should be 0.127mm. Inter-pair matching should be within 2.54cm. Max Length 241.3mm.

DisplayPort AUX CH intra-pair matching should be 0.127mm. Max length 330.2mm.

SOURCE: Calpella SFF DG Rev 1.5 (407364) and Family GPU DG-04202-001-v04.

MAX LENGTH OF DISPLAYPORT/TMDS TRACES: 13 INCHES.

## CPU Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
DMI_S2N	CPU_85D	DMI_S2N	DMI_S2N P<3:0>	5 12 87
DMI_S2N	CPU_85D	DMI_S2N	DMI_S2N N<3:0>	5 12 87
DMI_N2S	CPU_85D	DMI_N2S	DMI_N2S P<3:0>	5 12 87
DMI_N2S	CPU_85D	DMI_N2S	DMI_N2S N<3:0>	5 12 87
FDI_INT	CPU_50S	CPU_AGTL	FDI_INT	5 12
FDI_CSYNCR	CPU_50S	CPU_AGTL	FDI_CSYNCR	5 12
CLK_DMI	CPU_85D	CLK_DMI	DMI_CLK100M CPU P	4 11
CLK_DMI	CPU_85D	CLK_DMI	DMI_CLK100M CPU N	4 11
CPU_CLK135_PLL	CPU_85D	CLK_PCIE	CPU_CLK135M DPLLREF N	6 11
CPU_CLK135_PLL	CPU_85D	CLK_PCIE	CPU_CLK135M DPLLREF P	6 11
CPU_CLK135_PLL	CPU_85D	CLK_PCIE	CPU_CLK135M DPLLSS N	6 11
CPU_CLK135_PLL	CPU_85D	CLK_PCIE	CPU_CLK135M DPLLSS P	6 11
CPU_EDP_COMP	CPU_27P4S	CPU_COMP	CPU EDP RCOMP	5
CPU_PEG_COMP	CPU_27P4S	CPU_COMP	CPU PEG RCOMP	5
CPU_CFG	CPU_45S	CPU_ITP	CPU CFG<19..0>	6 18 86

XDP_CLK_BCH	CLK_PCIE_85D	CLK_PCIE	NC ITPXDP CLK100MP	11 87
XDP_CLK_BCH	CLK_PCIE_85D	CLK_PCIE	NC ITPXDP CLK100MN	11 87
XDP_TDI	CPU_45S	CPU_ITP	XDP CPU TDI	6 18 86
XDP_TDO	CPU_45S	CPU_ITP	XDP CPU TDO	6 18 86
XDP_TMS	CPU_45S	CPU_ITP	XDP CPU TMS	6 18 86
XDP_TCK	CPU_45S	CPU_ITP	XDP CPU TCK	6 18 86
XDP_TRST_L	CPU_45S	CPU_ITP	XDP CRUPCH TRST_L	6 18 86
XDP_BPM	CPU_45S	CPU_ITP	XDP BPM L<3..0>	6 18
XDP_BPM_L	CPU_45S	CPU_ITP	XDP BPM L<7..4>	6 18
XDP_DBRESET_L	CPU_45S	CPU_ITP	XDP DBRESET_L	6 18 19
XDP_PRDY_L	CPU_45S	CPU_ITP	XDP CPU PRDY_L	6 18 86
XDP_PREQ_L	CPU_45S	CPU_ITP	XDP CPU PREQ_L	6 18 86
CPU_CATERR_L	CPU_45S	CPU_AGTL	CPU CATERR_L	6 40
CPU_PECI	CPU_45S	CPU_VID	CPU Peci	6 14 41
CPU_PROCHOT_L	CPU_45S	CPU_AGTL	CPU PROCHOT_L	6 40 41 58

CPU_PWRGD	CPU_45S	CPU_AGTL	CPU PWRGD	6 14 18
PM_THRMTRIP_L	CPU_45S	CPU_SMIL	PM THRMTRIP_L	6 14 41
PM_MEM_PWRGD	CPU_45S	CPU_AGTL	PM MEM_PWRGD	6 12 21
PM_SYNC	CPU_45S	CPU_AGTL	PM SYNC	6 12
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU SM_RCOMP<2..0>	6
CPU_VID	CPU_45S	CPU_VID	CPU VIDSOUT	8 58
CPU_VID	CPU_45S	CPU_VID	CPU VIDCLK	8 58
CPU_VID	CPU_45S	CPU_VID	CPU VIDALERT_L	8 58
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU VCCSENSE_P	8 58
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU VCCSENSE_N	9 58
CPU_MEM_VREF	MEM_12MIL		CPU DIMMA VREFDQ	7 22
CPU_MEM_VREF	MEM_12MIL		CPU DIMMB VREFDQ	7 22
CPU_MEM_VREF	MEM_PWR		PP0V75_S3 MEM VREFDQ_A	22 23 24 85 92
CPU_MEM_VREF	CPU_VREF		PP0V75_S3 MEM VREFDQ_B	22 25 26 85
CPU_MEM_VREF	MEM_PWR		PP0V75_S3 MEM VREFCA	22 23 24 25 26 85 89 92
CPU_MEM_VREF	MEM_PWR		PP0V75_S3 MEM VREFCA	22 23 24 25 26 85 89 92

PCIE_D2R_GPU	PEG_80D	PEG3_D2R	PEG D2R C P<7..0>	68 70
PCIE_D2R_GPU	PEG_80D	PEG3_D2R	PEG D2R C N<7..0>	68 70
PCIE_D2R_GPU	PEG_80D	PEG3_D2R	PEG D2R P<7..0>	70 85
PCIE_D2R_GPU	PEG_80D	PEG3_D2R	PEG D2R N<7..0>	70 85
PCIE_R2D_GPU	PEG_80D	PEG3_R2D	PEG R2D C P<7..0>	68 70 85
PCIE_R2D_GPU	PEG_80D	PEG3_R2D	PEG R2D C N<7..0>	68 70 85
PCIE_R2D_GPU	PEG_80D	PEG3_R2D	PEG R2D P<7..0>	70
PCIE_R2D_GPU	PEG_80D	PEG3_R2D	PEG R2D N<7..0>	70

PCIE_D2R_SSD	CPU_85D	PEG3_D2R	PCIE SSD D2R P<3..0>	5 34 85
PCIE_D2R_SSD	CPU_85D	PEG3_D2R	PCIE SSD D2R N<3..0>	5 34 85
PCIE_R2D_SSD	CPU_85D	PEG3_R2D	PCIE SSD R2D C P<3..0>	5 34 85
PCIE_R2D_SSD	CPU_85D	PEG3_R2D	PCIE SSD R2D C N<3..0>	5 34 85
PCIE_R2D_SSD	CPU_85D	PEG3_R2D	PCIE SSD R2D P<3..0>	34
PCIE_R2D_SSD	CPU_85D	PEG3_R2D	PCIE SSD R2D N<3..0>	34

PCIE_D2R_TBT	CPU_85D	PEG_D2R	PCIE TBT D2R P<3..0>	5 28 85
PCIE_D2R_TBT	CPU_85D	PEG_D2R	PCIE TBT D2R N<3..0>	5 28 85
PCIE_D2R_TBT	CPU_85D	PEG_D2R	PCIE TBT D2R C P<3..0>	28 87
PCIE_D2R_TBT	CPU_85D	PEG_D2R	PCIE TBT D2R C N<3..0>	28 87
PCIE_R2D_TBT	CPU_85D	PEG_R2D	PCIE TBT R2D P<3..0>	28 87
PCIE_R2D_TBT	CPU_85D	PEG_R2D	PCIE TBT R2D N<3..0>	28 87
PCIE_R2D_TBT	CPU_85D	PEG_R2D	PCIE TBT R2D C P<3..0>	5 28 85
PCIE_R2D_TBT	CPU_85D	PEG_R2D	PCIE TBT R2D C N<3..0>	5 28 85

## DP AUX NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
DP_IG_AUX	DP_85D	DISPLAYPORT	DPA_IG_AUX_CH_P	12 83 85
DP_IG_AUX	DP_85D	DISPLAYPORT	DPA_IG_AUX_CH_N	12 83 85
DP_IG_AUX	DP_85D	DISPLAYPORT	DPB_IG_AUX_CH_P	12 83 85
DP_IG_AUX	DP_85D	DISPLAYPORT	DPB_IG_AUX_CH_N	12 83 85

## DP / HDMI NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
DP_TBT_ML0	DP_85D	DISPLAYPORT	DP TBTSNK0 ML C P<3..0>	28 76 97
DP_TBT_ML0	DP_85D	DISPLAYPORT	DP TBTSNK0 ML C N<3..0>	28 76 97
DP_TBT_ML0	DP_85D	DISPLAYPORT	DP TBTSNK0 ML P<3..0>	28 97
DP_TBT_ML0	DP_85D	DISPLAYPORT	DP TBTSNK0 ML N<3..0>	28 97
DP_TBT_ML1	DP_85D	DISPLAYPORT	DP TBTSNK1 ML C P<3..0>	28 76 97
DP_TBT_ML1	DP_85D	DISPLAYPORT	DP TBTSNK1 ML C N<3..0>	28 76 97
DP_TBT_ML1	DP_85D	DISPLAYPORT	DP TBTSNK1 ML P<3..0>	28 97
DP_TBT_ML1	DP_85D	DISPLAYPORT	DP TBTSNK1 ML N<3..0>	28 97
TBTSNK_AUXCH	DP_85D		DP TBTSNK0 AUXCH_P	28 97
TBTSNK_AUXCH	DP_85D		DP TBTSNK0 AUXCH_N	28 97
TBTSNK_AUXCH	DP_85D		DP TBTSNK0 AUXCH_C_P	28 83 97
TBTSNK_AUXCH	DP_85D		DP TBTSNK0 AUXCH_C_N	28 83 97
TBTSNK_AUXCH	DP_85D		DP TBTSNK1 AUXCH_P	28 97
TBTSNK_AUXCH	DP_85D		DP TBTSNK1 AUXCH_N	28 97
TBTSNK_AUXCH	DP_85D		DP TBTSNK1 AUXCH_C_P	28 83 97
TBTSNK_AUXCH	DP_85D		DP TBTSNK1 AUXCH_C_N	28 83 97

SYNC MASTER=CLEAN X305 PEG SYNC DATE=02/18/2014

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### SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
SATA_37SE	*	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE
SATA_45SE	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA_2SAME	*	=3X_DIELECTRIC	?
SATA_TXRX	*	=6X_DIELECTRIC	?
SATA_2OTHER	*	=4X_DIELECTRIC	?
SATA_RCOMP	*	=6X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA_2SAME	TOP,BOTTOM	=4X_DIELECTRIC	?
SATA_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
SATA_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?
SATA_RCOMP	TOP,BOTTOM	=10X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SATA_*	=SAME	*	SATA_2SAME
SATA_R2D	SATA_D2R	*	SATA_TXRX
SATA_*	*	*	SATA_2OTHER

### USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_USB_RBIAS	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
USB_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=4X_DIELECTRIC	?
USB_RBIAS	*	=6X_DIELECTRIC	?
BT_WAKE	*	=4X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=6X_DIELECTRIC	?
USB_RBIAS	TOP,BOTTOM	=10X_DIELECTRIC	?
BT_WAKE	TOP,BOTTOM	=6X_DIELECTRIC	?

### USB 3.0 INTERFACE CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB3_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_2SAME	*	=3X_DIELECTRIC	?
USB3_TXRX	*	=6X_DIELECTRIC	?
USB3_2OTHER	*	=4X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_2SAME	TOP,BOTTOM	=4X_DIELECTRIC	?
USB3_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
USB3_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB3_*	=SAME	*	USB3_2SAME
USB3_R2D	USB3_D2R	*	USB3_TXRX
USB3_*	*	*	USB3_2OTHER

### System Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CLK_25M_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=4X_DIELECTRIC	?
CLK_25M	*	=5X_DIELECTRIC	?


NOTE: 25MHz system clocks very sensitive to noise.  
NOTE: Latest Intel DG calls out 50ohms SE for sys clocks

### PCH Net Properties

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
SATA_85D	SATA_R5D	SATA_R2D	NC SATA A R2D CP 11 87
SATA_85D	SATA_85D	SATA_R2D	NC SATA A R2D CN 11 87
SATA_85D	SATA_D2R	SATA_D2R	NC SATA A D2RP 11 87
SATA_85D	SATA_D2R	SATA_D2R	NC SATA A D2RN 11 87
SATA_85D	SATA_R2D	SATA_R2D	NC SATA B R2D CP 11 87
SATA_85D	SATA_R2D	SATA_R2D	NC SATA B R2D CN 11 87
SATA_85D	SATA_D2R	SATA_D2R	NC SATA B D2RP 11 87
SATA_85D	SATA_D2R	SATA_D2R	NC SATA B D2RN 11 87
PCH_SATA_RCOMP	SATA_45SE	SATA_RCOMP	PCH SATA RCOMP 11
USB_EXTN	USB_85D	USB	USB EXTN P 13 37
USB_EXTN	USB_85D	USB	USB EXTN N 13 37
USB_EXTN	USB_85D	USB	USB EXTN MUXED P 37
USB_EXTN	USB_85D	USB	USB EXTN MUXED N 37
USB_EXTN	USB_85D	USB	USB LT1 P 37
USB_EXTN	USB_85D	USB	USB LT1 N 37
USB_NC	USB_85D	USB	NC USB EXTCP 13 87
USB_NC	USB_85D	USB	NC USB EXTCN 13 87
USB_NC	USB_85D	USB	NC USB SDP 13 87
USB_NC	USB_85D	USB	NC USB SDN 13 87
CPU_45S	CPU_45S	CPU_ITP	SMC DEBUGPRT RX L 37 40 41
CPU_45S	CPU_45S	CPU_ITP	SMC DEBUGPRT TX L 37 40 41
USB_SMC	USB_85D	USB	NC USB SMCN 87
USB_SMC	USB_85D	USB	NC USB SMCN 87
USB_NC	USB_85D	USB	NC USB 6P 13 87
USB_NC	USB_85D	USB	NC USB 6N 13 87
USB_NC	USB_85D	USB	NC USB 7P 13 87
USB_NC	USB_85D	USB	NC USB 7N 13 87
USB_EXTB	USB_85D	USB	USB EXTB P 13 81 86
USB_EXTB	USB_85D	USB	USB EXTB N 13 81 86
USB_NC	USB_85D	USB	NC USB EXTDN 13 87
USB_BT	USB_85D	USB	USB BT P 13 33
USB_BT	USB_85D	USB	USB BT N 13 33
USB_BT	USB_85D	USB	USB BT CONN P 33 86
USB_BT	USB_85D	USB	USB BT CONN N 33 86
USB_NC	USB_85D	USB	NC USB IRP 13 87
USB_NC	USB_85D	USB	NC USB IRN 13 87
USB_TPAD	USB_85D	USB	USB TPAD P 13 38 86
USB_TPAD	USB_85D	USB	USB TPAD N 13 38 86
USB_TPAD	USB_85D	USB	USB TPAD R P
USB_TPAD	USB_85D	USB	USB TPAD R N
PCH_USB_RBIAS	PCH_USB_RBIAS	USB_RBIAS	PCH USB RBIAS 13
USB3_EXTN_RX	USB_85D	USB3_D2R	USB3 EXTN D2R P 13 37
USB3_EXTN_RX	USB_85D	USB3_D2R	USB3 EXTN D2R N 13 37
USB3_EXTN	USB_85D	USB3_D2R	USB3 EXTN D2R C P
USB3_EXTN	USB_85D	USB3_D2R	USB3 EXTN D2R C N
USB3_EXTN_TX	USB_85D	USB3_R2D	USB3 EXTN R2D P 37
USB3_EXTN_TX	USB_85D	USB3_R2D	USB3 EXTN R2D N 37
USB3_EXTN	USB_85D	USB3_R2D	USB3 EXTN R2D C P 13 37
USB3_EXTN	USB_85D	USB3_R2D	USB3 EXTN R2D C N 13 37
USB3_EXTB_RX	USB_85D	USB3_D2R	USB3 EXTB D2R P 13 81 86
USB3_EXTB_RX	USB_85D	USB3_D2R	USB3 EXTB D2R N 13 81 86
USB3_EXTB	USB_85D	USB3_D2R	USB3 EXTB D2R C P
USB3_EXTB	USB_85D	USB3_D2R	USB3 EXTB D2R C N
USB3_EXTB_TX	USB_85D	USB3_R2D	USB3 EXTB R2D P 81 86
USB3_EXTB_TX	USB_85D	USB3_R2D	USB3 EXTB R2D N 81 86
USB3_EXTB	USB_85D	USB3_R2D	USB3 EXTB R2D C P 13 81
USB3_EXTB	USB_85D	USB3_R2D	USB3 EXTB R2D C N 13 81
NC_USB3	USB_85D	USB3_D2R	NC USB3 EXTC D2RP 13 87
NC_USB3	USB_85D	USB3_D2R	NC USB3 EXTC D2RN 13 87
NC_USB3	USB_85D	USB3_R2D	NC USB3 EXTC R2D CP 13 87
NC_USB3	USB_85D	USB3_R2D	NC USB3 EXTC R2D CN 13 87
NC_USB3	USB_85D	USB3_D2R	NC USB3 EXTD D2RP 13 87
NC_USB3	USB_85D	USB3_D2R	NC USB3 EXTD D2RN 13 87
NC_USB3	USB_85D	USB3_R2D	NC USB3 EXTD R2D CP 13 87
NC_USB3	USB_85D	USB3_R2D	NC USB3 EXTD R2D CN 13 87

### Clock Net Properties

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
SYSCLK_CLK32K_RTC	CLK_SLOW_45S	CLK_SLOW	SYSCLK CLK32K RTC 11 19
SYSCLK_CLK25M_SB	CLK_25M_45S	CLK_25M	SYSCLK CLK25M SB 11 19
SYSCLK_CLK25M_CAM	CLK_25M_45S	CLK_25M	SYSCLK CLK25M SB R 11
SYSCLK_CLK25M_CAM	CLK_25M_45S	CLK_25M	SYSCLK CLK25M CAMERA 19 36
SYSCLK_CLK25M_TBT	CLK_25M_45S	CLK_25M	SYSCLK CLK25M TBT 19 28
SYSCLK_CLK25M_TBT	CLK_25M_45S	CLK_25M	SYSCLK CLK25M TBT R 28

SYNC MASTER=SIDLE J45		SYNC DATE=12/10/2012	
PAGE TITLE			
PCH Constraints 1			
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## LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

## SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

## HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFFAIR PRIMARY GAP	DIFFFAIR NECK GAP
HDA_45G	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

## SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_45G	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?
SPI3X	*	=3x_DIELECTRIC	?

## PCH Single Net Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_45G	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCH_SE	*	=2x_DIELECTRIC	?	PCH_SE	TOP,BOTTOM	=3x_DIELECTRIC	?

## PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
CLK_PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_2SAME	*	=2X_DIELECTRIC	?	PCIE_2SAME	TOP,BOTTOM	=4X_DIELECTRIC	?
PCIE_TXRX	*	=6X_DIELECTRIC	?	PCIE_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
PCIE_2OTHER	*	=4X_DIELECTRIC	?	PCIE_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?
PCIE_2CLK	*	=7X_DIELECTRIC	?	PCIE_2CLK	TOP,BOTTOM	=10X_DIELECTRIC	?
PCIECLK_2OTHER	*	=7X_DIELECTRIC	?	PCIECLK_2OTHER	TOP,BOTTOM	=10X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_*	=SAME	*	PCIE_2SAME
PCIE_R2D	PCIE_D2R	*	PCIE_TXRX
PCIE_*	*	*	PCIE_2OTHER
PCIE_*	CLK_*	*	PCIE_2CLK
CLK_PCIE	*	*	PCIECLK_2OTHER

## PCH Net Properties

ELECTRICAL_CONSTRAINT_SET		PHYSICAL		SPACING		
	LEC_AD	LEC_45S	LEC	LPC_AD<3..0>		13 40 82
	LPC_FRAME_L	LEC_45S	LEC	LPC_FRAME_L		13 40 82
	SMBUS_PCH_CLK	SMB_45S	SMB	SMBUS_PCH_CLK		13 18 43 81 85 86
	SMBUS_PCH_DATA	SMB_45S	SMB	SMBUS_PCH_DATA		13 18 43 81 85 86
	SMBUS_PCH_0_CLK	SMB_45S	SMB	SML_PCH_0_CLK		13 43
	SMBUS_PCH_0_DATA	SMB_45S	SMB	SML_PCH_0_DATA		13 43
	SMBUS_PCH_1_CLK	SMB_45S	SMB	SML_PCH_1_CLK		13 43
	SMBUS_PCH_1_DATA	SMB_45S	SMB	SML_PCH_1_DATA		13 43
	HDA_BIT_CLK	HDA_45S	HDA	HDA_BIT_CLK		11 52
		HDA_45S	HDA	HDA_BIT_CLK_R		11
	HDA_SYNC	HDA_45S	HDA	HDA_SYNC		11 52
		HDA_45S	HDA	HDA_SYNC_R		11
		HDA_45S	HDA	HDA_RST_R_L		11
	HDA_RST_L	HDA_45S	HDA	HDA_RST_L		11 52
	HDA_SDIN0	HDA_45S	HDA	HDA_SDIN0		11 52
	HDA_SDIN0_R	HDA_45S	HDA	CS4208_HDA_SDOUT0_R		92
	HDA_SDOUT	HDA_45S	HDA	HDA_SDOUT		11 52
		HDA_45S	HDA	HDA_SDOUT_R		11 19
	USB3_SD_R2D	USB3_85D	USB3_R2D	USB3_SD_R2D_C_P		13 20 81 86
	USB3_SD_R2D	USB3_85D	USB3_R2D	USB3_SD_R2D_C_N		13 20 81 86
	USB3_SD_D2R	USB3_85D	USB3_D2R	USB3_SD_D2R_P		13 20 81 86
	USB3_SD_D2R	USB3_85D	USB3_D2R	USB3_SD_D2R_N		13 20 81 86


PCIE AP R2D	PCIE_R5D	PCIE_R2D	PCIE AP R2D P	13 86
PCIE AP R2D	PCIE_R5D	PCIE_R2D N	PCIE AP R2D N	13 86
PCIE_R5D	PCIE_R5D	PCIE_R2D	PCIE AP R2D C P	13 83
PCIE_R5D	PCIE_R5D	PCIE_R2D	PCIE AP R2D C N	13 83
PCIE_R5D	PCIE_R5D	PCIE_R2D	PCIE AP R2D PI P	
PCIE_R5D	PCIE_R5D	PCIE_R2D	PCIE AP R2D PI N	
PCIE AP D2R	PCIE_R5D	PCIE_D2R	PCIE AP D2R P	13 20 3
PCIE AP D2R	PCIE_R5D	PCIE_D2R	PCIE AP D2R N	13 20 3
PCIE_R5D	PCIE_R5D	PCIE_D2R	PCIE AP D2R PI P	86
PCIE_R5D	PCIE_R5D	PCIE_D2R	PCIE AP D2R PI N	86
PCIE_CAMERA_R2D	PCIE_R5D	PCIE_R2D	PCIE CAMERA R2D P	35 36
PCIE_CAMERA_R2D	PCIE_R5D	PCIE_R2D	PCIE CAMERA R2D N	35 36
PCIE_R5D	PCIE_R5D	PCIE_R2D	PCIE CAMERA R2D C P	13 36
PCIE_R5D	PCIE_R5D	PCIE_R2D	PCIE CAMERA R2D C N	13 36
PCIE_CAMERA_D2R	PCIE_R5D	PCIE_D2R	PCIE CAMERA D2R P	13 20 3
PCIE_CAMERA_D2R	PCIE_R5D	PCIE_D2R	PCIE CAMERA D2R N	13 20 3
PCIE_R5D	PCIE_R5D	PCIE_D2R	PCIE CAMERA D2R C P	35 36
PCIE_R5D	PCIE_R5D	PCIE_D2R	PCIE CAMERA D2R C N	35 36

		CLK_LPC_45S	CLK_LPC	LPC CLK33M SMC R	11	19
	PCH_LPC_CLK0	CLK_LPC_45S	CLK_LPC	LPC CLK33M SMC	19	40
PCIE0		CLK_LPC_45S	CLK_LPC	NC LPC CLK33M LPCPLUS R	11	87
	PCIE_CLK100M	CPUI_45S	CLK_PCIE	PCIE CLK33M PCIIIN	11	11
	PCIE_CLK100M	CPUI_45S	CLK_PCIE	PCH CLK14P3M REFCLK	11	
	PCIE_CLK100M	CPUI_45S	CLK_PCIE	PCH CLK33M PCIOUT	11	19
	PCIE_CLK100M_PCH	CLK_PCIE_85D	CLK_PCIE	PCIE CLK100M PCH P	11	
	PCIE_CLK100M_PCH	CLK_PCIE_85D	CLK_PCIE	PCIE CLK100M PCH N	11	
	PCIE_CLK100M_TBT	CLK_PCIE_85D	CLK_PCIE	PCIE CLK100M TBT P	11	28
	PCIE_CLK100M_TBT	CLK_PCIE_85D	CLK_PCIE	PCIE CLK100M TBT N	11	28
	PCIE_CLK100M_DOT	CLK_PCIE_85D	CLK_PCIE	PCH CLK96M DOT P	11	
	PCIE_CLK100M_DOT	CLK_PCIE_85D	CLK_PCIE	PCH CLK96M DOT N	11	
	PCIE_CLK100M_SATA	PCIE_85D	CLK_PCIE	PCH CLK100M SATA P	11	
	PCIE_CLK100M_SATA	PCIE_85D	CLK_PCIE	PCH CLK100M SATA N	11	
	PCIE_CLK100M_ENET	PCIE_85D	CLK_PCIE	PCIE CLK100M SD P	11	
	PCIE_CLK100M_ENET	PCIE_85D	CLK_PCIE	PCIE CLK100M SD N	11	
	PCIE_CLK100M_AP	PCIE_85D	CLK_PCIE	PCIE CLK100M AP P	11	33
	PCIE_CLK100M_AP	PCIE_85D	CLK_PCIE	PCIE CLK100M AP N	11	33
PCIE0		PCIE_85D	CLK_PCIE	PCIE CLK100M AP CONN P	31	86
		PCIE_85D	CLK_PCIE	PCIE CLK100M AP CONN N	31	86
	PCIE_CLK100M_S2	CLK_PCIE_85D	CLK_PCIE	PCIE CLK100M CAMERA P	31	36
	PCIE_CLK100M_S2	CLK_PCIE_85D	CLK_PCIE	PCIE CLK100M CAMERA N	31	36
PCIE0		CLK_PCIE_85D	CLK_PCIE	PCIE CLK100M CAMERA C P	35	36
PCIE0		CLK_PCIE_85D	CLK_PCIE	PCIE CLK100M CAMERA C N	35	36

PCIE_CLK100M_FW	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_SSD_P	11.34
PCIE_CLK100M_SSD_N	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_SSD_N	11.34
PCIE_CLK100M_GPU	CLK_PCIE_85D	CLK_PCIE	PEG_CLK100M_P	11.79
PEG_CLK100M_N	CLK_PCIE_85D	CLK_PCIE	PEG_CLK100M_N	11.79

### PCH Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		
		PHYSICAL	SPACING	
R388	PCH_EM_NET	PCH_45S	PCH_SE	PCH INTRUDER L 11
R397	PCH_EM_NET	PCH_45S	PCH_SE	PCH INTVRMEN L 11
R398	PCH_EM_NET	PCH_45S	PCH_SE	PCH DSWVRMEN 12
R399	PCH_EM_NET	PCH_45S	PCH_SE	PCH SRTCRST L 11
R400	PCH_EM_NET	PCH_45S	PCH_SE	PM RSMRST L 12 67 86
R401	PCH_EM_NET	PCH_45S	PCH_SE	PM SYSRST L 12 19 40 86
R402	PCH_EM_NET	PCH_45S	PCH_SE	PM PCH PWROK 12 19 86 91
R403	PCH_EM_NET	PCH_45S	PCH_SE	PM PCH PWROK 12 19 86 91
R404	PCH_EM_NET	PCH_45S	PCH_SE	PM DSW PWROK 12 40 86
R405	PCH_EM_NET	PCH_45S	PCH_SE	PM PCH SYS PWROK 12 18 19 40 86
R406	PCH_EM_NET	PCH_45S	PCH_SE	PM PWRBTN L 12 18 40
R407	PCH_EM_NET	PCH_45S	PCH_SE	PM THRMTrip L R 14 41 42
R408	PCH_PCIE_WAKE	PCH_45S	PCH_SE	PCIE WAKE L 12 33 35 86
R409	PCH_EM_NET	PCH_45S	PCH_SE	PCH RCIN L 14
R389	SPI_MLB	SPT_45S	SPT3X	SPI ALT CLK
R390	SPI_MLB	SPT_45S	SPT	SPI CLK 60
R391	SPI_MLB	SPT_45S	SPT	SPI CLK R 13 50
R392	SPI_MLB	SPT_45S	SPT3X	SPI MLB CLK 60
R393	SPI_MLB	SPT_45S	SPT3X	SPI SMC CLK 40 50
R394	SPI_MLB	SPT_45S	SPT3X	SPI ALT CS L
R395	SPI_MLB	SPT_45S	SPT	SPI CS0 L 60
R396	SPI_MLB	SPT_45S	SPT	SPI CS0 R L 13 50
R397	SPI_MLB	SPT_45S	SPT3X	SPI MLB CS L 60
R398	SPI_MLB	SPT_45S	SPT3X	SPI SMC CS L 40 50
R399	SPI_MLB	SPT_45S	SPT3X	SPI ALT IO1 MISO
R400	SPI_MLB	SPT_45S	SPT	SPI MISO 13 50
R401	SPI_MLB	SPT_45S	SPT	SPI MISO R 60
R402	SPI_MLB	SPT_45S	SPT3X	SPI MLB IO1 MISO 60
R403	SPI_MLB	SPT_45S	SPT3X	SPI SMC MISO 40 50
R404	SPI_MLB	SPT_45S	SPT3X	SPI ALT IO0 MOSI
R405	SPI_MLB	SPT_45S	SPT	SPI MOSI 60
R406	SPI_MLB	SPT_45S	SPT	SPI MOSI R 13 50
R407	SPI_MLB	SPT_45S	SPT3X	SPI MLB IO0 MOSI 60
R408	SPI_MLB	SPT_45S	SPT3X	SPI SMC MOSI 40 50
R409	SPI_MLB_IO2	SPT_45S	SPT3X	SPI IO<2> 13 50
R410	SPI_MLB_IO2	SPT_45S	SPT3X	SPI MLB IO2 WP L 60
R411	SPI_MLB_IO2	SPT_45S	SPT3X	SPI ALT IO2 WP L
R412	SPI_MLB_IO3	SPT_45S	SPT3X	SPI IO<3> 13 50
R413	SPI_MLB_IO3	SPT_45S	SPT3X	SPI MLB IO3 HOLD L 60
R414	SPI_MLB_IO3	SPT_45S	SPT3X	SPI ALT IO3 HOLD L
R415	SPI_TPAD	SPT_45S	SPT	TPAD SPI SCLK 38 85
R416	SPI_TPAD_CS	SPT_45S	SPT	TPAD SPI CS L 38 85
R417	SPI_TPAD	SPT_45S	SPT	TPAD SPI MISO 38 85
R418	SPI_TPAD	SPT_45S	SPT	TPAD SPI MOSI 38 85

SYNCH MASTER=CLEAN X305 PEG		SYNCH DATE=02/18/2014	
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## Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_37S	*	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=STANDARD	=STANDARD
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_72D	*	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF
MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

## Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_DATA2SELF	*	=2x_DIELECTRIC	?
MEM_DQS2OWNDATA	*	=2x_DIELECTRIC	?
MEM_CMD2CMD	*	=2x_DIELECTRIC	?
MEM_CMD2CTRL	*	=2x_DIELECTRIC	?
MEM_CTRL2CTRL	*	=2x_DIELECTRIC	?
MEM_CLK2CLK	*	=4x_DIELECTRIC	?
MEM_2OTHERMEM	*	=4x_DIELECTRIC	?
MEM_2PWR	*	=2x_DIELECTRIC	?
MEM_2GND	*	=2x_DIELECTRIC	?
MEM_2OTHER	*	=6x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_DATA2SELF	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_DQS2OWNDATA	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_CMD2CMD	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_CMD2CTRL	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_CTRL2CTRL	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_CLK2CLK	TOP,BOTTOM	=8x_DIELECTRIC	?
MEM_2OTHERMEM	TOP,BOTTOM	=8x_DIELECTRIC	?
MEM_2PWR	TOP,BOTTOM	=4x_DIELECTRIC	?
MEM_2GND	TOP,BOTTOM	=4x_DIELECTRIC	?
MEM_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

## Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DATA_*	*	*	MEM_2OTHER
MEM_*_DQS_*	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CLK	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DATA_*	=SAME	*	MEM_DATA2SELF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_CTRL	*	MEM_CMD2CTRL
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CLK	MEM_CLK	*	MEM_CLK2CLK
MEM_*	MEM_*	*	MEM_2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_A_DQS_0	MEM_A_DATA_0	*	MEM_DQS2OWNDATA
MEM_A_DQS_1	MEM_A_DATA_1	*	MEM_DQS2OWNDATA
MEM_A_DQS_2	MEM_A_DATA_2	*	MEM_DQS2OWNDATA
MEM_A_DQS_3	MEM_A_DATA_3	*	MEM_DQS2OWNDATA
MEM_A_DQS_4	MEM_A_DATA_4	*	MEM_DQS2OWNDATA
MEM_A_DQS_5	MEM_A_DATA_5	*	MEM_DQS2OWNDATA
MEM_A_DQS_6	MEM_A_DATA_6	*	MEM_DQS2OWNDATA
MEM_A_DQS_7	MEM_A_DATA_7	*	MEM_DQS2OWNDATA
MEM_B_DQS_0	MEM_B_DATA_0	*	MEM_DQS2OWNDATA
MEM_B_DQS_1	MEM_B_DATA_1	*	MEM_DQS2OWNDATA
MEM_B_DQS_2	MEM_B_DATA_2	*	MEM_DQS2OWNDATA
MEM_B_DQS_3	MEM_B_DATA_3	*	MEM_DQS2OWNDATA
MEM_B_DQS_4	MEM_B_DATA_4	*	MEM_DQS2OWNDATA
MEM_B_DQS_5	MEM_B_DATA_5	*	MEM_DQS2OWNDATA
MEM_B_DQS_6	MEM_B_DATA_6	*	MEM_DQS2OWNDATA
MEM_B_DQS_7	MEM_B_DATA_7	*	MEM_DQS2OWNDATA

### DDR3 (Memory Down):

DQ signals should be matched within 0.508mm of associated DQS pair  
DQS intra-pair matching should be within 0.127mm, no inter-pair matching requirement.  
DQS to clock matching should be within [CLK-139.73mm] and [CLK-30.48mm].  
CLK intra-pair matching should be within 0.127mm, inter-pair matching should be within 0.508mm.  
CONTROL signals should be matched within [CLK-2.54mm] to [CLK+0mm] of CLK pairs.  
A/BA/CMD signals should be matched within [CLK-2.54mm] to [CLK+2.54mm] of CLK pairs.  
DQ/DQS/A/BA/cmd signal spacing is 4x dielectric, CLK is 5x dielectric.  
Maximum length of any signal from die pad to first DRAM device is 139.7mm max, to last DRAM device is 194.31mm max.

SOURCE: Double checked with Doc#486985 Chief River SFF Platform DG: Memory Down  
SOURCE: Need to re-confirm CRW DG for memory down (Intel not yet provided)

## Memory to Power Spacing


NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_PWR	MEM_*	*	MEM_2PWR
MEM_PWR	*	*	DEFAULT

## Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	MEM_*	*	MEM_2GND

## Memory Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE	
		PHYSICAL	SPACING
	MEM_A_CLK0	MEM_72D	MEM_CLK
	MEM_A_CLK0	MEM_72D	MEM_CLK
FF00	MEM_A_CLK1	MEM_72D	MEM_CLK
FF00	MEM_A_CLK1	MEM_72D	MEM_CLK
	MEM_A_CNTL0	MEM_40S	MEM_CTRL
FF00	MEM_A_CNTL1	MEM_40S	MEM_CTRL
FF00	MEM_A_CNTL0	MEM_40S	MEM_CTRL
FF00	MEM_A_CNTL1	MEM_40S	MEM_CTRL
FF00	MEM_A_CNTL0	MEM_40S	MEM_CTRL
FF00	MEM_A_CNTL1	MEM_40S	MEM_CTRL
	MEM_A_CMD	MEM_40S	MEM_CMD
	MEM_A_CMD	MEM_40S	MEM_CMD
	MEM_A_CMD	MEM_40S	MEM_CMD
	MEM_A_CMD	MEM_40S	MEM_CMD
	MEM_A_CMD	MEM_40S	MEM_CMD
	MEM_A_DATA_0	MEM_45S	MEM_A_DATA_0
	MEM_A_DATA_1	MEM_45S	MEM_A_DATA_1
	MEM_A_DATA_2	MEM_45S	MEM_A_DATA_2
	MEM_A_DATA_3	MEM_45S	MEM_A_DATA_3
	MEM_A_DATA_4	MEM_45S	MEM_A_DATA_4
	MEM_A_DATA_5	MEM_45S	MEM_A_DATA_5
	MEM_A_DATA_6	MEM_45S	MEM_A_DATA_6
FF00	MEM_A_DATA_7	MEM_45S	MEM_A_DATA_7
FF00	MEM_A_DQS0	MEM_85D	MEM_A_DQS_0
	MEM_A_DQS0	MEM_85D	MEM_A_DQS_0
	MEM_A_DQS1	MEM_85D	MEM_A_DQS_1
	MEM_A_DQS1	MEM_85D	MEM_A_DQS_1
	MEM_A_DQS2	MEM_85D	MEM_A_DQS_2
	MEM_A_DQS2	MEM_85D	MEM_A_DQS_2
	MEM_A_DQS3	MEM_85D	MEM_A_DQS_3
	MEM_A_DQS3	MEM_85D	MEM_A_DQS_3
	MEM_A_DQS4	MEM_85D	MEM_A_DQS_4
	MEM_A_DQS4	MEM_85D	MEM_A_DQS_4
	MEM_A_DQS5	MEM_85D	MEM_A_DQS_5
	MEM_A_DQS5	MEM_85D	MEM_A_DQS_5
FF00	MEM_A_DQS6	MEM_85D	MEM_A_DQS_6
FF00	MEM_A_DQS6	MEM_85D	MEM_A_DQS_6
FF00	MEM_A_DQS7	MEM_85D	MEM_A_DQS_7
FF00	MEM_A_DQS7	MEM_85D	MEM_A_DQS_7
	MEM_B_CLK0	MEM_72D	MEM_CLK
	MEM_B_CLK0	MEM_72D	MEM_CLK
FF00	MEM_B_CLK1	MEM_72D	MEM_CLK
FF00	MEM_B_CLK1	MEM_72D	MEM_CLK
	MEM_B_CNTL0	MEM_40S	MEM_CTRL
FF00	MEM_B_CNTL1	MEM_40S	MEM_CTRL
FF00	MEM_B_CNTL0	MEM_40S	MEM_CTRL
FF00	MEM_B_CNTL1	MEM_40S	MEM_CTRL
FF00	MEM_B_CNTL0	MEM_40S	MEM_CTRL
FF00	MEM_B_CNTL1	MEM_40S	MEM_CTRL
	MEM_B_CMD	MEM_40S	MEM_CMD
	MEM_B_CMD	MEM_40S	MEM_CMD
	MEM_B_CMD	MEM_40S	MEM_CMD
	MEM_B_CMD	MEM_40S	MEM_CMD
	MEM_B_DATA_0	MEM_45S	MEM_B_DATA_0
	MEM_B_DATA_1	MEM_45S	MEM_B_DATA_1
	MEM_B_DATA_2	MEM_45S	MEM_B_DATA_2
	MEM_B_DATA_3	MEM_45S	MEM_B_DATA_3
	MEM_B_DATA_4	MEM_45S	MEM_B_DATA_4
	MEM_B_DATA_5	MEM_45S	MEM_B_DATA_5
	MEM_B_DATA_6	MEM_45S	MEM_B_DATA_6
	MEM_B_DATA_7	MEM_45S	MEM_B_DATA_7
	MEM_B_DQS0	MEM_85D	MEM_B_DQS_0
	MEM_B_DQS0	MEM_85D	MEM_B_DQS_0
	MEM_B_DQS1	MEM_85D	MEM_B_DQS_1
	MEM_B_DQS1	MEM_85D	MEM_B_DQS_1
	MEM_B_DQS2	MEM_85D	MEM_B_DQS_2
	MEM_B_DQS2	MEM_85D	MEM_B_DQS_2
	MEM_B_DQS3	MEM_85D	MEM_B_DQS_3
	MEM_B_DQS3	MEM_85D	MEM_B_DQS_3
	MEM_B_DQS4	MEM_85D	MEM_B_DQS_4
	MEM_B_DQS4	MEM_85D	MEM_B_DQS_4
	MEM_B_DQS5	MEM_85D	MEM_B_DQS_5
	MEM_B_DQS5	MEM_85D	MEM_B_DQS_5
FF00	MEM_B_DQS6	MEM_85D	MEM_B_DQS_6
FF00	MEM_B_DQS6	MEM_85D	MEM_B_DQS_6
FF00	MEM_B_DQS7	MEM_85D	MEM_B_DQS_7
FF00	MEM_B_DQS7	MEM_85D	MEM_B_DQS_7
		MEM_PWR	PP0V75_S3 MEM VREFD0 A
FF00		MEM_PWR	PP0V75_S3 MEM VREFCA
FF00		MEM_PWR	PP1V35_S3 MEM

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## DisplayPort Signal Constraints

NOTE: DisplayPort Physical/Spacing Constraints provided by Chipset or GPU page.

## Thunderbolt SPI Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBT_SPI_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBT_SPI	*	=2x_DIELECTRIC	?

## Thunderbolt/DP Connector Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBTD_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SOURCE: Bill Cornelius's Thunderbolt Routing Notes

## TBT\_DP Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBTD_P_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTD_P_2SAME	*	=3X_DIELECTRIC	?
TBTD_P_TXRX	*	=6X_DIELECTRIC	?
TBTD_P_2OTHER	*	=4X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
TBTDP_*	=SAME	*	TBTDP_2SAME
TBTDP_R2D	TBTDP_D2R	*	TBTDP_TXRX
TBTDP_*	*	*	TBTDP_2OTHER

## Thunderbolt/DP Net Properties


ELECTRICAL CONSTRAINT_SBT		NET_TYPE		
		PHYSICAL	SPACING	
	TBT_A_R2D	TBTDP_R5D	TBTDP_R2D	TBT A R2D C P<1..0>
	TBT_A_R2D	TBTDP_R5D	TBTDP_R2D	TBT A R2D C N<1..0>
	TBT_A_R2D	TBTDP_R5D	TBTDP_R2D	TBT A R2D P<1..0>
	TBT_A_R2D	TBTDP_R5D	TBTDP_R2D	TBT A R2D N<1..0>
	DP_A_LSX_ML	DP_R5D	DISPLAYPORT	DP TBTPA ML C P<1>
	DP_A_LSX_ML	DP_R5D	DISPLAYPORT	DP TBTPA ML C N<1>
	DP_A_LSX_ML	DP_R5D	DISPLAYPORT	DP TBTPA ML P<1>
	DP_A_LSX_ML	DP_R5D	DISPLAYPORT	DP TBTPA ML N<1>
	DP_A_LSX_ML	DP_R5D	DISPLAYPORT	DP A LSX ML P<1>
	DP_A_LSX_ML	DP_R5D	DISPLAYPORT	DP A LSX ML N<1>
	DP_TBTTPA_ML	DP_R5D	DISPLAYPORT	DP TBTTPA ML C P<3>
	DP_TBTTPA_ML	DP_R5D	DISPLAYPORT	DP TBTTPA ML C N<3>
	DP_TBTTPA_ML	DP_R5D	DISPLAYPORT	DP TBTTPA ML P<3>
	DP_TBTTPA_ML	DP_R5D	DISPLAYPORT	DP TBTTPA ML N<3>
	TBT_A_D2R0	TBTDP_R5D	TBTDP_D2R	TBT A D2R C P<0>
	TBT_A_D2R0	TBTDP_R5D	TBTDP_D2R	TBT A D2R C N<0>
	TBT_A_D2R0	TBTDP_R5D	TBTDP_D2R	TBT A D2R P<0>
	TBT_A_D2R0	TBTDP_R5D	TBTDP_D2R	TBT A D2R N<0>
	TBT_A_D2R1	TBTDP_R5D	TBTDP_D2R	TBT A D2R C P<1>
	TBT_A_D2R1	TBTDP_R5D	TBTDP_D2R	TBT A D2R C N<1>
	TBT_A_D2R1	TBTDP_R5D	TBTDP_D2R	TBT A D2R P<1>
	TBT_A_D2R1	TBTDP_R5D	TBTDP_D2R	TBT A D2R N<1>
	TBT_A_D2R1	TBTDP_R5D	TBTDP_D2R	TBT A D2R1 AUXDDC P
	TBT_A_D2R1	TBTDP_R5D	TBTDP_D2R	TBT A D2R1 AUXDDC N
	TBT_A_AUXCH	DP_R5D		DP TBTTPA AUXCH C P
	TBT_A_AUXCH	DP_R5D		DP TBTTPA AUXCH C N
	TBT_A_AUXCH	DP_R5D		DP TBTTPA AUXCH P
	TBT_A_AUXCH	DP_R5D		DP TBTTPA AUXCH N
	TBT_B_R2D	TBTDP_R5D	TBTDP_R2D	TBT B R2D C P<1..0>
	TBT_B_R2D	TBTDP_R5D	TBTDP_R2D	TBT B R2D C N<1..0>
	TBT_B_R2D	TBTDP_R5D	TBTDP_R2D	TBT B R2D P<1..0>
	TBT_B_R2D	TBTDP_R5D	TBTDP_R2D	TBT B R2D N<1..0>
	DP_B_LSX_ML	DP_R5D	DISPLAYPORT	DP TBTTPB ML C P<1>
	DP_B_LSX_ML	DP_R5D	DISPLAYPORT	DP TBTTPB ML C N<1>
	DP_B_LSX_ML	DP_R5D	DISPLAYPORT	DP TBTTPB ML P<1>
	DP_B_LSX_ML	DP_R5D	DISPLAYPORT	DP TBTTPB ML N<1>
	DP_B_LSX_ML	DP_R5D	DISPLAYPORT	DP B LSX ML P<1>
	DP_B_LSX_ML	DP_R5D	DISPLAYPORT	DP B LSX ML N<1>
	DP_TBTTPB_ML	DP_R5D	DISPLAYPORT	DP TBTTPB ML C P<3>
	DP_TBTTPB_ML	DP_R5D	DISPLAYPORT	DP TBTTPB ML C N<3>
	DP_TBTTPB_ML	DP_R5D	DISPLAYPORT	DP TBTTPB ML P<3>
	DP_TBTTPB_ML	DP_R5D	DISPLAYPORT	DP TBTTPB ML N<3>
	TBT_B_D2R0	TBTDP_R5D	TBTDP_D2R	TBT B D2R C P<0>
	TBT_B_D2R0	TBTDP_R5D	TBTDP_D2R	TBT B D2R C N<0>
	TBT_B_D2R0	TBTDP_R5D	TBTDP_D2R	TBT B D2R P<0>
	TBT_B_D2R0	TBTDP_R5D	TBTDP_D2R	TBT B D2R N<0>
	TBT_B_D2R1	TBTDP_R5D	TBTDP_D2R	TBT B D2R C P<1>
	TBT_B_D2R1	TBTDP_R5D	TBTDP_D2R	TBT B D2R C N<1>
	TBT_B_D2R1	TBTDP_R5D	TBTDP_D2R	TBT B D2R P<1>
	TBT_B_D2R1	TBTDP_R5D	TBTDP_D2R	TBT B D2R1 AUXDDC P
	TBT_B_D2R1	TBTDP_R5D	TBTDP_D2R	TBT B D2R1 AUXDDC N
	TBT_B_AUXCH	DP_R5D		DP TBTTPB AUXCH C P
	TBT_B_AUXCH	DP_R5D		DP TBTTPB AUXCH C N
	TBT_B_AUXCH	DP_R5D		DP TBTTPB AUXCH P
	TBT_B_AUXCH	DP_R5D		DP TBTTPB AUXCH N

Only used on dual-port hosts.

## Thunderbolt IC Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		
		PHYSICAL	SPACING	
		DP_85D	DISPLAYPORT	DP_TBTSRC ML C P<3..0>
		DP_85D	DISPLAYPORT	DP_TBTSRC ML C N<3..0>
		DP_85D	DISPLAYPORT	DP_TBTSRC AUXCH C P
		DP_85D	DISPLAYPORT	DP_TBTSRC AUXCH C N
	TBT_SPT_CLK	TBT_SPT_45S	TBT_SPT	TBT_SPT_CLK
	TBT_SPT_MOST	TBT_SPT_45S	TBT_SPT	TBT_SPT MOSI
	TBT_SPT_MISO	TBT_SPT_45S	TBT_SPT	TBT_SPT MISO
	TBT_SPT_CS_L	TBT_SPT_45S	TBT_SPT	TBT_SPT CS L

Only used on hosts supporting Thunderbolt video-in

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### MIPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM_LINE_WIDTH	MINIMUM_NECK_WIDTH	MAXIMUM_NECK_LENGTH	DIFFPAIR_PRIMARY_GAP	DIFFPAIR_NECK_GAP
MIPI_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE_SPACING	WEIGHT
MIPI_20THER	*	=4X_DIELECTRIC	?
MIPI_2CLK	*	=6X_DIELECTRIC	?
MIPICLK_20THER	*	=7X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MIPI_DATA	*	*	MIPI_20THER
MIPI_DATA	CLK_MIPI	*	MIPI_2CLK
CLK_MIPI	*	*	MIPICLK_20THER

### Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM_LINE_WIDTH	MINIMUM_NECK_WIDTH	MAXIMUM_NECK_LENGTH	DIFFPAIR_PRIMARY_GAP	DIFFPAIR_NECK_GAP
S2_MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
S2_MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

### Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE_SPACING	WEIGHT
S2_DATA2SELF	*	=2x_DIELECTRIC	?
S2_DQS2OWNDATA	*	=2x_DIELECTRIC	?
S2_CMD2CMD	*	=2x_DIELECTRIC	?
S2_CMD2CTRL	*	=2x_DIELECTRIC	?
S2_CTRL2CTRL	*	=2x_DIELECTRIC	?
S2_20THERMEM	*	=4x_DIELECTRIC	?
S2MEM_2PWR	*	=2x_DIELECTRIC	?
S2MEM_2GND	*	=2x_DIELECTRIC	?
S2MEM_2OTHER	*	=6x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE_SPACING	WEIGHT
S2_DATA2SELF	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_DQS2OWNDATA	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CMD2CMD	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CMD2CTRL	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CTRL2CTRL	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_20THERMEM	TOP,BOTTOM	=6x_DIELECTRIC	?
S2MEM_2PWR	TOP,BOTTOM	=4x_DIELECTRIC	?
S2MEM_2GND	TOP,BOTTOM	=4x_DIELECTRIC	?
S2MEM_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

### Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_DATA*	*	*	S2MEM_20THER
S2_MEM_DQS*	*	*	S2MEM_20THER
S2_MEM_CMD	*	*	S2MEM_20THER
S2_MEM_CTRL	*	*	S2MEM_20THER
S2_MEM_CLK	*	*	S2MEM_20THER
S2_MEM_DATA*	=SAME	*	S2_DATA2SELF
S2_MEM_CMD	S2_MEM_CMD	*	S2_CMD2CMD
S2_MEM_CMD	S2_MEM_CTRL	*	S2_CMD2CTRL
S2_MEM_CTRL	S2_MEM_CTRL	*	S2_CTRL2CTRL
S2_MEM_*	S2_MEM_*	*	S2_20THERMEM

### Memory to Power Spacing


NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_PWR	S2_MEM_*	*	S2MEM_2PWR
S2_MEM_PWR	*	*	DEFAULT

### Memory to GND Spacing

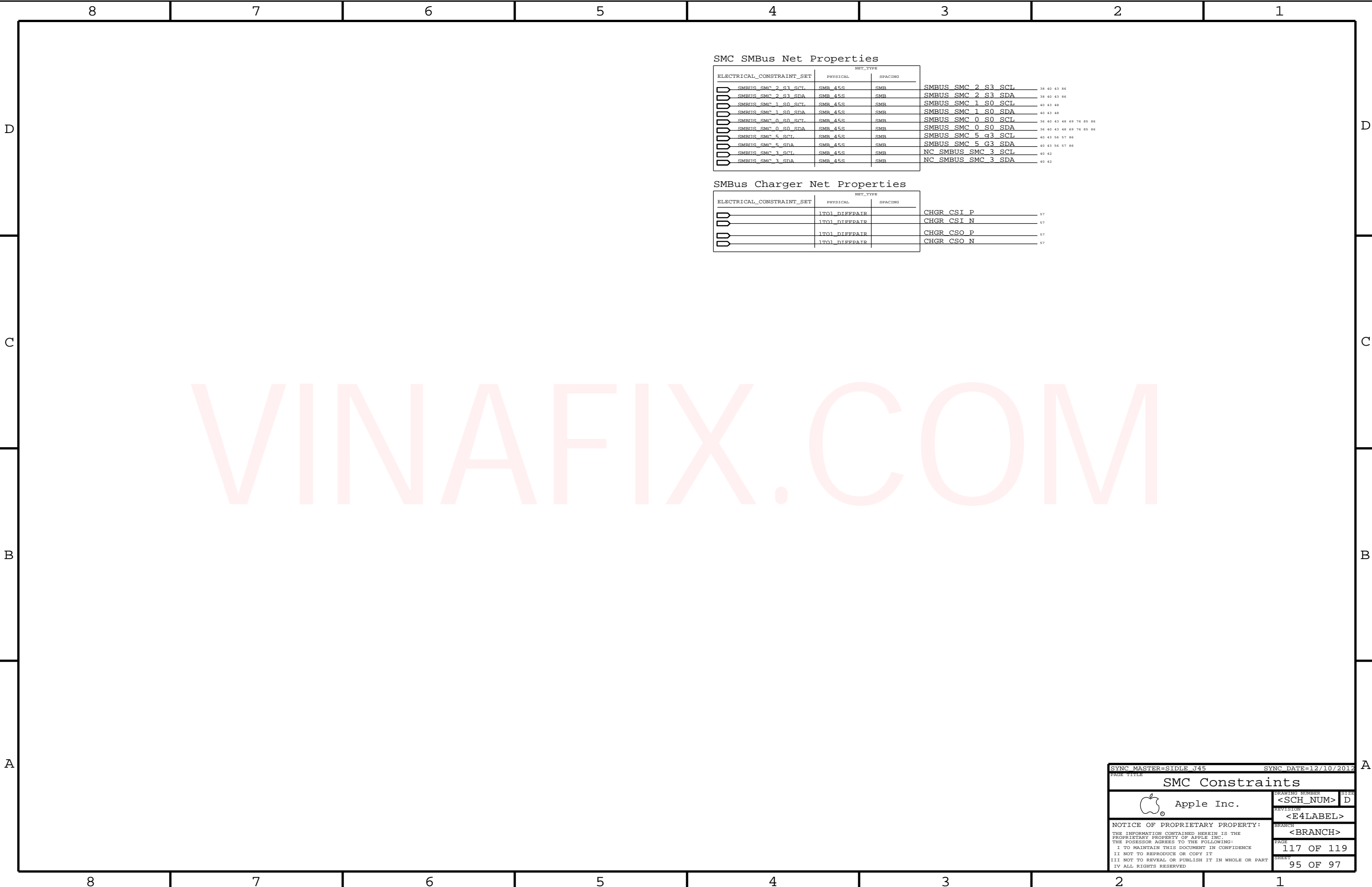
NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	S2_MEM_*	*	S2MEM_2GND

### Camera Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
S2_MEM_CLK	S2_MEM_85D	S2_MEM_CLK	MEM_CAM_CLK_P 35 36
S2_MEM_CLK	S2_MEM_85D	S2_MEM_CLK	MEM_CAM_CLK_N 35 36
S2_MEM_CNTRL	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CKE 35 36
S2_MEM_CNTRL	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CS_L 35 36
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_ODT 36
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CAS_L 35 36
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_RAS_L 35 36
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_WE_L 35 36
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<0> 35 36
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<1> 35 36
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<2> 35 36
S2_MEM_DQS0	S2_MEM_85D	S2_MEM_DQS0	MEM_CAM_DQS_P<0> 35 36
S2_MEM_DQS0	S2_MEM_85D	S2_MEM_DQS0	MEM_CAM_DQS_N<0> 35 36
S2_MEM_DQS1	S2_MEM_85D	S2_MEM_DQS1	MEM_CAM_DQS_P<1> 35 36
S2_MEM_DQS1	S2_MEM_85D	S2_MEM_DQS1	MEM_CAM_DQS_N<1> 35 36
S2_MEM_DATA_0	S2_MEM_45S	S2_MEM_DATA0	MEM_CAM_DM<0> 35 36
S2_MEM_DATA_1	S2_MEM_45S	S2_MEM_DATA1	MEM_CAM_DM<1> 35 36
S2_MEM_A	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_A<14..0> 35 36
S2_MEM_DATA_0	S2_MEM_45S	S2_MEM_DATA0	MEM_CAM_DQ<7..0> 35 36
S2_MEM_DATA_1	S2_MEM_45S	S2_MEM_DATA1	MEM_CAM_DQ<15..8> 35 36
MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_P 35 36
MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_N 35 36
MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_CONN_P 36 86
MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_CONN_N 36 86
MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_P 35 36
MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_N 35 36
MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_CONN_P 36 86
MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_CONN_N 36 86
		S2_MEM_PWR	PP1V35_CAM 35 36
		S2_MEM_PWR	PP0V675_CAM_VREF 35 36
		S2_MEM_PWR	PP0V675_MEM_CAM_VREFCA 36
		S2_MEM_PWR	PP0V675_MEM_CAM_VREFDQ 36

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PAGE TITLE			
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SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
SMBUS_SMC_2_S3_SCL	SMB_45S	SMB	SMBUS_SMC_2_S3_SCL	38 40 43 86
SMBUS_SMC_2_S3_SDA	SMB_45S	SMB	SMBUS_SMC_2_S3_SDA	38 40 43 86
SMBUS_SMC_1_S0_SCL	SMB_45S	SMB	SMBUS_SMC_1_S0_SCL	40 43 48
SMBUS_SMC_1_S0_SDA	SMB_45S	SMB	SMBUS_SMC_1_S0_SDA	40 43 48
SMBUS_SMC_0_S0_SCL	SMB_45S	SMB	SMBUS_SMC_0_S0_SCL	36 40 43 48 69 76 85 86
SMBUS_SMC_0_S0_SDA	SMB_45S	SMB	SMBUS_SMC_0_S0_SDA	36 40 43 48 69 76 85 86
SMBUS_SMC_5_SCL	SMB_45S	SMB	SMBUS_SMC_5_S3_SCL	40 43 56 57 86
SMBUS_SMC_5_SDA	SMB_45S	SMB	SMBUS_SMC_5_G3_SDA	40 43 56 57 86
SMBUS_SMC_3_SCL	SMB_45S	SMB	NC SMBUS_SMC_3_SCL	40 42
SMBUS_SMC_3_SDA	SMB_45S	SMB	NC SMBUS_SMC_3_SDA	40 42

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
1T01_DIEFFPAIR	1T01_DIEFFPAIR		CHGR_CSI_P	57
1T01_DIEFFPAIR	1T01_DIEFFPAIR		CHGR_CSI_N	57
1T01_DIEFFPAIR	1T01_DIEFFPAIR		CHGR_CSO_P	57
1T01_DIEFFPAIR	1T01_DIEFFPAIR		CHGR_CSO_N	57

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SYNC\_DATE=12/10/2012

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NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	GRID	*	GRID_P2MH
CPU_VCCSENSE	GRID	*	GRID_P2MH

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLR_PCIE	QND	*	QND_P2004 <small>https://www.semicore.com/technical_documents/Products/PCIe/PCIe%20QND%20P2004.pdf</small>
QND	PCIE_*	*	QND_P2004 <small>https://www.semicore.com/technical_documents/Products/PCIe/PCIe%20QND%20P2004.pdf</small>
QND	SATA_*	*	QND_P2004 <small>https://www.semicore.com/technical_documents/Products/PCIe/PCIe%20QND%20P2004.pdf</small>
USB	QND	*	QND_P2004 <small>https://www.semicore.com/technical_documents/Products/PCIe/PCIe%20QND%20P2004.pdf</small>
CLR_PCIE	SR_POWER	*	PWR_P2004 <small>https://www.semicore.com/technical_documents/Products/PCIe/PCIe%20PWR%20P2004.pdf</small>
SR_POWER	SATA_*	*	PWR_P2004 <small>https://www.semicore.com/technical_documents/Products/PCIe/PCIe%20PWR%20P2004.pdf</small>
USB	SR_POWER	*	PWR_P2004 <small>https://www.semicore.com/technical_documents/Products/PCIe/PCIe%20PWR%20P2004.pdf</small>

CCBB

## A

A

diff:

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x42

DCBA

## GDDR5 Frame Buffer Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
GDDR5_45R50SE	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	12.7 MM	=STANDARD	=STANDARD
GDDR5_45SE	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
GDDR5_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GDDR5_CLK	*	=5x_DIELECTRIC	?
GDDR5_CMD	*	=3x_DIELECTRIC	?
GDDR5_DATA	*	=3x_DIELECTRIC	?
GDDR5_EDC	*	=7x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GDDR5_CLK	TOP, BOTTOM	=5x_DIELECTRIC	?
GDDR5_CMD	TOP, BOTTOM	=4x_DIELECTRIC	?
GDDR5_DATA	TOP, BOTTOM	=5x_DIELECTRIC	?
GDDR5_EDC	TOP, BOTTOM	=7x_DIELECTRIC	?

GDDR5\_CMD spacing can be relaxed to 2x per AMD recommendation for x32\_4.5G config.

### Breakout Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GDDR5_*	*	BGA	GDDR5_BGA

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GDDR5_BGA	*	= 1.3x_DIELECTRIC	?

## GDDR5 FB A Net Properties

ELECTRICAL_CONSTRAINT_SET		SET_TYPE		DYNAMIC	
		PHYSICAL			
R938	FB_A0_CLK	GDDR5_80D	GDDR5_CLK	FB A0 CLK P	72 76
R939	FB_A0_CLK	GDDR5_80D	GDDR5_CLK	FB A0 CLK N	72 76
R940	FB_A1_CLK	GDDR5_80D	GDDR5_CLK	FB A1 CLK P	72 76
R941	FB_A1_CLK	GDDR5_80D	GDDR5_CLK	FB A1 CLK N	72 76
R942	FB_A0_CMD	GDDR5_45SE	GDDR5_CMD	FB A0 A<8..0>	72 76
R943	FB_A1_CMD	GDDR5_45SE	GDDR5_CMD	FB A1 A<8..0>	72 76
R944	FB_A0_CMD	GDDR5_45SE	GDDR5_CMD	FB A0 ABI L	72 76
R945	FB_A1_CMD	GDDR5_45SE	GDDR5_CMD	FB A1 ABI L	72 76
R946	FB_A0_CMD	GDDR5_45SE	GDDR5_CMD	FB A0 RAS L	72 76
R947	FB_A1_CMD	GDDR5_45SE	GDDR5_CMD	FB A1 RAS L	72 76
R948	FB_A0_CMD	GDDR5_45SE	GDDR5_CMD	FB A0 CAS L	72 76
R949	FB_A1_CMD	GDDR5_45SE	GDDR5_CMD	FB A1 CAS L	72 76
R950	FB_A0_CMD	GDDR5_45SE	GDDR5_CMD	FB A0 WE L	72 76
R951	FB_A1_CMD	GDDR5_45SE	GDDR5_CMD	FB A1 WE L	72 76
R952	FB_A0_CMD	GDDR5_45SE	GDDR5_CMD	FB A0 CKE L	72 76
R953	FB_A1_CMD	GDDR5_45SE	GDDR5_CMD	FB A1 CKE L	72 76
R954	FB_A0_CMD	GDDR5_45SE	GDDR5_CMD	FB A0 CS L	72 76
R955	FB_A1_CMD	GDDR5_45SE	GDDR5_CMD	FB A1 CS L	72 76
R956	FB_A0_EDC0	GDDR5_45SE	GDDR5_EDC	FB A0 EDC<0>	72 76
R957	FB_A0_EDC1	GDDR5_45SE	GDDR5_EDC	FB A0 EDC<1>	72 76
R958	FB_A0_EDC2	GDDR5_45SE	GDDR5_EDC	FB A0 EDC<2>	72 76
R959	FB_A0_EDC3	GDDR5_45SE	GDDR5_EDC	FB A0 EDC<3>	72 76
R960	FB_A1_EDC0	GDDR5_45SE	GDDR5_EDC	FB A1 EDC<0>	72 76
R961	FB_A1_EDC1	GDDR5_45SE	GDDR5_EDC	FB A1 EDC<1>	72 76
R962	FB_A1_EDC2	GDDR5_45SE	GDDR5_EDC	FB A1 EDC<2>	72 76
R963	FB_A1_EDC3	GDDR5_45SE	GDDR5_EDC	FB A1 EDC<3>	72 76
R964	FB_A0_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB A0 DBI L<0>	72 76
R965	FB_A0_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB A0 DBI L<1>	72 76
R966	FB_A0_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB A0 DBI L<2>	72 76
R967	FB_A0_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB A0 DBI L<3>	72 76
R968	FB_A1_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB A1 DBI L<0>	72 76
R969	FB_A1_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB A1 DBI L<1>	72 76
R970	FB_A1_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB A1 DBI L<2>	72 76
R971	FB_A1_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB A1 DBI L<3>	72 76
R972	FB_A0_WCLK0	GDDR5_80D	GDDR5_CLK	FB A0 WCLK P<0>	72 76
R973	FB_A0_WCLK0	GDDR5_80D	GDDR5_CLK	FB A0 WCLK N<0>	72 76
R974	FB_A0_WCLK1	GDDR5_80D	GDDR5_CLK	FB A0 WCLK P<1>	72 76
R975	FB_A0_WCLK1	GDDR5_80D	GDDR5_CLK	FB A0 WCLK N<1>	72 76
R976	FB_A1_WCLK0	GDDR5_80D	GDDR5_CLK	FB A1 WCLK P<0>	72 76
R977	FB_A1_WCLK0	GDDR5_80D	GDDR5_CLK	FB A1 WCLK N<0>	72 76
R978	FB_A1_WCLK1	GDDR5_80D	GDDR5_CLK	FB A1 WCLK P<1>	72 76
R979	FB_A1_WCLK1	GDDR5_80D	GDDR5_CLK	FB A1 WCLK N<1>	72 76
R980	FB_A0_DO_BYTE0	GDDR5_45SE	GDDR5_DATA	FB A0 DO<7..0>	72 76
R981	FB_A0_DO_BYTE1	GDDR5_45SE	GDDR5_DATA	FB A0 DO<15..8>	72 76
R982	FB_A0_DO_BYTE2	GDDR5_45SE	GDDR5_DATA	FB A0 DO<23..16>	72 76
R983	FB_A0_DO_BYTE3	GDDR5_45SE	GDDR5_DATA	FB A0 DO<31..24>	72 76
R984	FB_A1_DO_BYTE0	GDDR5_45SE	GDDR5_DATA	FB A1 DO<7..0>	72 76
R985	FB_A1_DO_BYTE1	GDDR5_45SE	GDDR5_DATA	FB A1 DO<15..8>	72 76
R986	FB_A1_DO_BYTE2	GDDR5_45SE	GDDR5_DATA	FB A1 DO<23..16>	72 76
R987	FB_A1_DO_BYTE3	GDDR5_45SE	GDDR5_DATA	FB A1 DO<31..24>	72 76
R988	FB_A0_CMD_R	GDDR5_45SE	GDDR5_CMD	FB A0 RESET L	72 76
R989	FB_A1_CMD_R	GDDR5_45SE	GDDR5_CMD	FB A1 RESET L	72 76









## GDDR5 FB B Net Properties


ELECTRICAL_CONSTRAINT_SET		NET_TYPE		
		FUNCTION	FUNCTION	
FE00	FB_B0_CLK	GDDR5_80D	GDDR5_CLK	FB B0 CLK P
FE00	FB_B0_CLK	GDDR5_80D	GDDR5_CLK	FB B0 CLK N
FE00	FB_B1_CLK	GDDR5_80D	GDDR5_CLK	FB B1 CLK P
FE00	FB_B1_CLK	GDDR5_80D	GDDR5_CLK	FB B1 CLK N
FE00	FB_B0_CMD	GDDR5_45SE	GDDR5_CMD	FB B0 A<8...0>
FE00	FB_B1_CMD	GDDR5_45SE	GDDR5_CMD	FB B1 A<8...0>
FE00	FB_B0_CMD	GDDR5_45SE	GDDR5_CMD	FB B0 ABI L
FE00	FB_B1_CMD	GDDR5_45SE	GDDR5_CMD	FB B1 ABI L
FE00	FB_B0_CMD	GDDR5_45SE	GDDR5_CMD	FB B0 RAS L
FE00	FB_B1_CMD	GDDR5_45SE	GDDR5_CMD	FB B1 RAS L
FE00	FB_B0_CMD	GDDR5_45SE	GDDR5_CMD	FB B0 CAS L
FE00	FB_B1_CMD	GDDR5_45SE	GDDR5_CMD	FB B1 CAS L
FE00	FB_B0_CMD	GDDR5_45SE	GDDR5_CMD	FB B0 WE L
FE00	FB_B1_CMD	GDDR5_45SE	GDDR5_CMD	FB B1 WE L
FE00	FB_B0_CMD	GDDR5_45SE	GDDR5_CMD	FB B0 CKE L
FE00	FB_B1_CMD	GDDR5_45SE	GDDR5_CMD	FB B1 CKE L
FE00	FB_B0_CMD	GDDR5_45SE	GDDR5_CMD	FB B0 CS L
FE00	FB_B1_CMD	GDDR5_45SE	GDDR5_CMD	FB B1 CS L
FE00	FB_B0_EDC0	GDDR5_45SE	GDDR5_EDC	FB B0 EDC<0>
FE00	FB_B0_EDC1	GDDR5_45SE	GDDR5_EDC	FB B0 EDC<1>
FE00	FB_B0_EDC2	GDDR5_45SE	GDDR5_EDC	FB B0 EDC<2>
FE00	FB_B0_EDC3	GDDR5_45SE	GDDR5_EDC	FB B0 EDC<3>
FE00	FB_B1_EDC0	GDDR5_45SE	GDDR5_EDC	FB B1 EDC<0>
FE00	FB_B1_EDC1	GDDR5_45SE	GDDR5_EDC	FB B1 EDC<1>
FE00	FB_B1_EDC2	GDDR5_45SE	GDDR5_EDC	FB B1 EDC<2>
FE00	FB_B1_EDC3	GDDR5_45SE	GDDR5_EDC	FB B1 EDC<3>
FE00	FB_B0_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB B0 DBI L<0>
FE00	FB_B0_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB B0 DBI L<1>
FE00	FB_B0_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB B0 DBI L<2>
FE00	FB_B0_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB B0 DBI L<3>
FE00	FB_B1_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB B1 DBI L<0>
FE00	FB_B1_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB B1 DBI L<1>
FE00	FB_B1_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB B1 DBI L<2>
FE00	FB_B1_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB B1 DBI L<3>
FE00	FB_B0_WCLK0	GDDR5_80D	GDDR5_CLK	FB B0 WCLK P<0>
FE00	FB_B0_WCLK0	GDDR5_80D	GDDR5_CLK	FB B0 WCLK N<0>
FE00	FB_B0_WCLK1	GDDR5_80D	GDDR5_CLK	FB B0 WCLK P<1>
FE00	FB_B0_WCLK1	GDDR5_80D	GDDR5_CLK	FB B0 WCLK N<1>
FE00	FB_B1_WCLK0	GDDR5_80D	GDDR5_CLK	FB B1 WCLK P<0>
FE00	FB_B1_WCLK0	GDDR5_80D	GDDR5_CLK	FB B1 WCLK N<0>
FE00	FB_B1_WCLK1	GDDR5_80D	GDDR5_CLK	FB B1 WCLK P<1>
FE00	FB_B1_WCLK1	GDDR5_80D	GDDR5_CLK	FB B1 WCLK N<1>
FE00	FB_B0_DQ_BYT00	GDDR5_45SE	GDDR5_DATA	FB B0 DQ<7...0>
FE00	FB_B0_DQ_BYT11	GDDR5_45SE	GDDR5_DATA	FB B0 DQ<15...8>
FE00	FB_B0_DQ_BYT22	GDDR5_45SE	GDDR5_DATA	FB B0 DQ<23...16>
FE00	FB_B0_DQ_BYT33	GDDR5_45SE	GDDR5_DATA	FB B0 DQ<31...24>
FE00	FB_B1_DQ_BYT00	GDDR5_45SE	GDDR5_DATA	FB B1 DQ<7...0>
FE00	FB_B1_DQ_BYT11	GDDR5_45SE	GDDR5_DATA	FB B1 DQ<15...8>
FE00	FB_B1_DQ_BYT22	GDDR5_45SE	GDDR5_DATA	FB B1 DQ<23...16>
FE00	FB_B1_DQ_BYT33	GDDR5_45SE	GDDR5_DATA	FB B1 DQ<31...24>
FE00	FB_B0_CMD_R	GDDR5_45SE	GDDR5_CMD	FB B0 RESET L
FE00	FB_B1_CMD_R	GDDR5_45SE	GDDR5_CMD	FB B1 RESET L

## MUXGFX &amp; DP AUX MUX NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET		PROVIDED	DEMAND	DEMAND
DEMAND	DP_85D	DISPLAYPORT	DP INT ML C P<3..0>	69 82
DEMAND	DP_85D	DISPLAYPORT	DP INT ML C N<3..0>	69 82
DEMAND	DP_85D	DISPLAYPORT	DP INT ML F P<3..0>	69
DEMAND	DP_85D	DISPLAYPORT	DP INT ML F N<3..0>	69
DEMAND	DP_INT_ML	DP_85D	DP INT ML P<3..0>	69 86
DEMAND	DP_INT_ML	DP_85D	DP INT ML N<3..0>	69 86
DEMAND	DP_85D	DISPLAYPORT	DP INT AUXCH C P	69 82
DEMAND	DP_85D	DISPLAYPORT	DP INT AUXCH C N	69 82
DEMAND	DP_INT_AUXCH	DP_85D	DP INT AUX P	69 86
DEMAND	DP_INT_AUXCH	DP_85D	DP INT AUX N	69 86
DEMAND	DP_85D	DISPLAYPORT	DP INT EG AUX P	76 77 82
DEMAND	DP_85D	DISPLAYPORT	DP INT EG AUX N	76 77 82
DEMAND	DP_INT_ML	DP_85D	DP INT EG ML P<3..0>	76 82
DEMAND	DP_85D	DISPLAYPORT	DP INT EG ML N<3..0>	76 82
DEMAND	DP_85D	DISPLAYPORT	DP INT IG AUX P	5 82 85
DEMAND	DP_85D	DISPLAYPORT	DP INT IG AUX N	5 82 85
DEMAND	DP_INT_ML	DP_85D	DP INT IG ML P<3..0>	5 82 85
DEMAND	DP_85D	DISPLAYPORT	DP INT IG ML N<3..0>	5 82 85
DEMAND	DP_EG_AUX	DP_85D	DP TBTSNKO EG AUXCH P	76 77
DEMAND	DP_EG_AUX	DP_85D	DP TBTSNKO EG AUXCH N	76 77 81
DEMAND	DP_EG_AUX	DP_85D	DP TBTSNKL EG AUXCH P	76 77 83
DEMAND	DP_EG_AUX	DP_85D	DP TBTSNKL EG AUXCH N	76 77 83
DEMAND	TBTSNK_AUXCH	DP_85D	DP TBTSNKO AUXCH P	28 89
DEMAND	TBTSNK_AUXCH	DP_85D	DP TBTSNKO AUXCH N	28 89
DEMAND	DP_85D	DISPLAYPORT	DP TBTSNKO AUXCH C P	28 83 89
DEMAND	DP_85D	DISPLAYPORT	DP TBTSNKO AUXCH C N	28 83 89
DEMAND	TBTSNK_AUXCH	DP_85D	DP TBTSNKL AUXCH P	28 89
DEMAND	TBTSNK_AUXCH	DP_85D	DP TBTSNKL AUXCH N	28 89
DEMAND	DP_85D	DISPLAYPORT	DP TBTSNKL AUXCH C P	28 83 89
DEMAND	DP_85D	DISPLAYPORT	DP TBTSNKL AUXCH C N	28 83 89
DEMAND	DP_TBT_ML	DP_85D	DP TBTSNKO ML P<3..0>	28 89
DEMAND	DP_TBT_ML	DP_85D	DP TBTSNKO ML N<3..0>	28 89
DEMAND	DP_85D	DISPLAYPORT	DP TBTSNKO ML C P<3..0>	28 76 89
DEMAND	DP_85D	DISPLAYPORT	DP TBTSNKO ML C N<3..0>	28 76 89
DEMAND	DP_TBT_ML1	DP_85D	DP TBTSNKL ML P<3..0>	28 89
DEMAND	DP_TBT_ML1	DP_85D	DP TBTSNKL ML N<3..0>	28 89
DEMAND	DP_85D	DISPLAYPORT	DP TBTSNKL ML C P<3..0>	28 76 89
DEMAND	DP_85D	DISPLAYPORT	DP TBTSNKL ML C N<3..0>	28 76 89

## Kepler Net Properties

HDMI CONSTRAINT SET		NET TYPE	
	PHYSICAL	SPACING	
 HDMI	1-13 DIFFERENTIAL	GPU CLK TEST RC P	
 HDMI	1-13 DIFFERENTIAL	GPU CLK TEST RC N	
 HDMI GPU_CLK_TEST	1-13 DIFFERENTIAL	GPU CLK TEST P	
 HDMI GPU_CLK_TEST	1-13 DIFFERENTIAL	GPU CLK TEST N	
 HDMI_DATA	DP_85D	DISPLAYPORT	HDMI EG DATA P<2..0>
 HDMI_DATA	DP_85D	DISPLAYPORT	HDMI EG DATA N<2..0>
 HDMI_CLK	DP_85D	HDMI_CLK	HDMI EG CLK P
 HDMI_CLK	DP_85D	HDMI_CLK	HDMI EG CLK N

SYNC MASTER: J45G AMD		SYNC DATE: 07/01/2014	
PAGE TITLE			
GPU (AMD VENUS) Constraints			
	Apple Inc.	DRAWING NUMBER	SIZE
		<SCH_NUM>	D
		REVISION	
		<E4LABEL>	
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